

## Diamond vacuum field emission devices

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### Abstract

This article reports the development of (a) vertical and (b) lateral diamond vacuum field emission devices with excellent field emission characteristics. These diamond field emission devices, diode and triode, were fabricated using a self-aligning gate formation technique from silicon-on-insulator wafers using conventional silicon micropatterning and etching techniques. High emission current  $>0.1$  A was achieved from the vertical diamond field emission diode with an indented anode design. The gated diamond triode in vertical configuration displayed excellent transistor characteristics with high DC gain of  $\sim 800$  and large AC output voltage of  $\sim 100$  V p-p. Lateral diamond field emission diodes with cathode-anode spacing less than  $2\ \mu\text{m}$  were fabricated. The lateral diamond emitter exhibited a low turn-on voltage of  $\sim 5$  V and a high emission current of  $6\ \mu\text{A}$ . The low turn-on voltage (field  $\sim 3$  V/ $\mu\text{m}$ ) and high emission characteristics are the best of reported lateral field emitter structures. © 2004 Elsevier B.V. All rights reserved.

**Keywords:** Diamond; Field emission; High current; DC gain; Lateral field emitter

### 1. Introduction

Chemical vapor deposited (CVD) diamond or related carbon materials are excellent materials for electron field emitters because of their low or negative affinity (NEA) [1–3] and excellent mechanical and chemical properties like high hardness and ability to withstand ion bombardment. The NEA property of diamond, unlike other materials, is retained in a residual gas ambient [4,5]. In addition to these properties, diamond has the highest thermal conductivity and can have high electrical conductivity, enabling diamond devices to operate at high temperatures and high power. This makes diamond field emitters potentially advantageous in vacuum microelectronics.

We have developed micropatterned diamond pyramidal tips with nanometer sharpness and achieved self-aligned gated diamond field emitters. In this paper, we report the

development of (a) vertical and (b) lateral diamond field emission devices with excellent field emission characteristics. These diamond field emission devices were fabricated on silicon-on-insulator (SOI) substrate utilizing conventional silicon micropatterning, lift-off and etching techniques to define anode, gate and cathode. The versatility and practicality of this approach for fabricating diamond field emission devices is demonstrated.

### 2. Device fabrication

#### 2.1. Fabrication of vertical diamond field emitter arrays with self-aligned gate

The fabrication flow chart of the self-aligned gated diamond field emitter devices utilizing SOI-based wafer is shown in Fig. 1. The SOI wafer is comprised of a  $15\text{-}\mu\text{m}$ -thick Si active layer,  $1\text{-}\mu\text{m}$ -thick  $\text{SiO}_2$  layer (BOX) and  $525\text{-}\mu\text{m}$ -thick Si handle. A  $0.2\text{-}\mu\text{m}$ -thick  $\text{SiO}_2$  layer was then grown on the wafer surfaces. Inverted pyramidal

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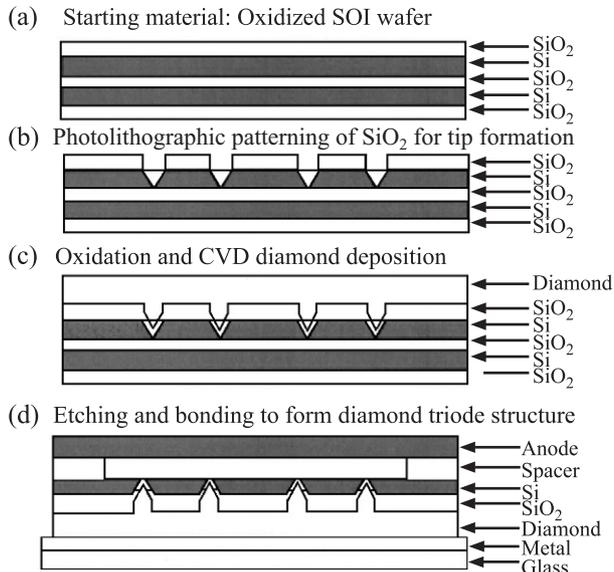


Fig. 1. Fabrication scheme of the self-aligned gated diamond field emitter triode.

cavities were then formed on the silicon active layer by photolithographic patterning and anisotropic etching of Si using KOH solution. The square patterns are sized such that complete inverted pyramidal cavities are formed within the Si active layer. Next, a SiO<sub>2</sub> layer was grown on the active Si layer to form the gate dielectric, which also produces a well-sharpened apex on the inverted pyramidal SiO<sub>2</sub> layer. Diamond was then deposited in the mold by plasma enhanced chemical vapor deposition technique (PECVD). The PECVD parameters are controlled to achieve small but deliberate sp<sup>2</sup> content in the diamond film. Next, the backside of the silicon was etched away and stopped at the embedded SiO<sub>2</sub> layer. Finally, the SiO<sub>2</sub> layer was etched and the sharpened diamond pyramidal apices exposed. The remaining SiO<sub>2</sub> and Si form the dielectric spacer and the gate, respectively. For the diode configuration the SiO<sub>2</sub> spacer and the remaining spacer were also etched to completely expose the diamond pyramids.

2.2. Fabrication of lateral diamond field emission arrays with co-built anode

The fabrication flow chart of the lateral diamond field emitter array with co-built anode is shown in Fig. 2. A 1-μm-thick SiO<sub>2</sub> layer was first grown onto the SOI wafer. Conventional photolithography was then performed to pattern the anode and cathode structures onto the SiO<sub>2</sub> layer. The exposed SiO<sub>2</sub> was etched away using BOE exposing the Si below. Next, electrically conductive diamond was preferentially grown on Si using bias enhanced PECVD. Conductivity of diamond was achieved by introducing trimethyl boron (TMB) gas in the plasma mixture for boron doping. The unwanted diamond that grew on SiO<sub>2</sub> was lifted-off by etching the SiO<sub>2</sub> using an HF etch

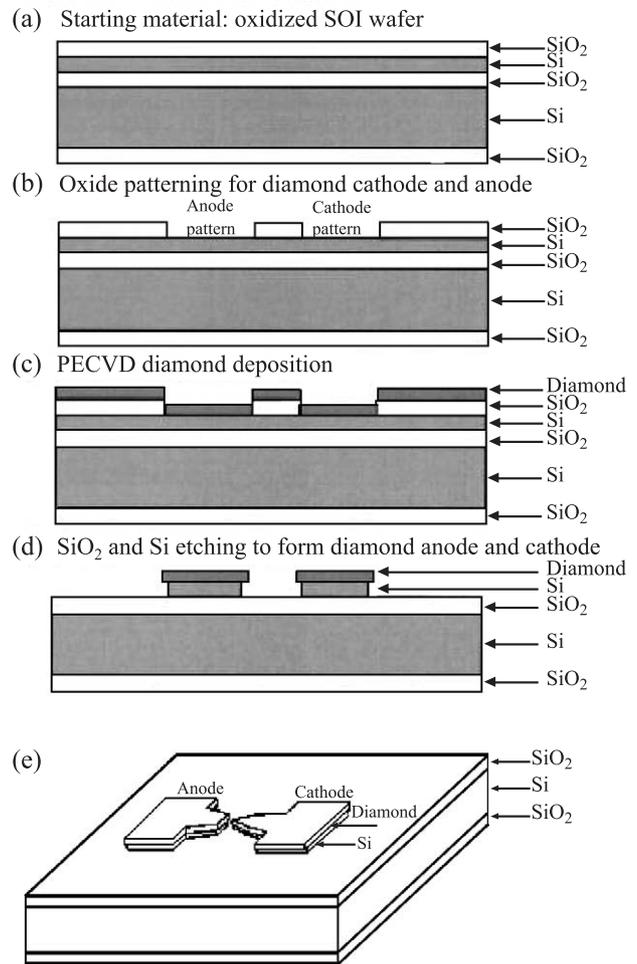


Fig. 2. Fabrication sequence for lateral diamond emitter utilizing SOI wafer.

in an ultrasonic bath. The patterned diamond layer was then used as a masking layer to etch Si to get the required spacing between the anode and cathode. The final structure

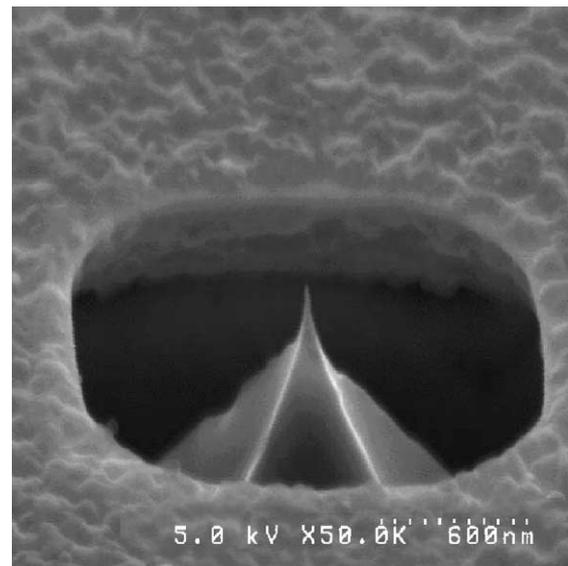


Fig. 3. SEM of vertical diamond VFET.

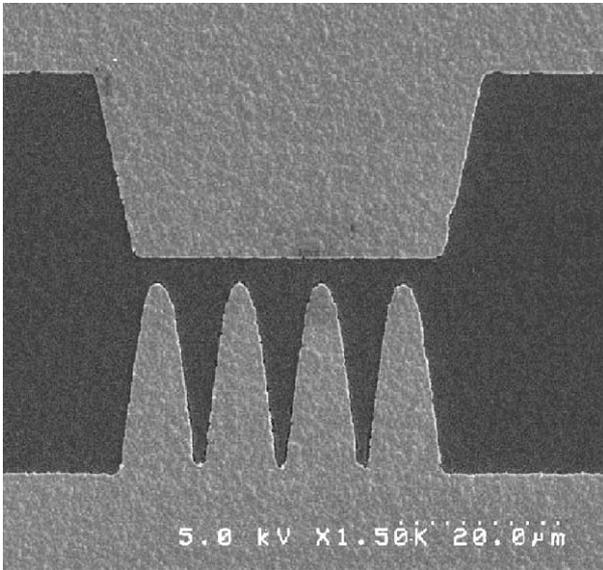


Fig. 4. SEM of lateral diamond field emission diode.

consists of patterned diamond anode and cathode, supported by a Si layer underneath, sitting on the SiO<sub>2</sub> layer on the Si substrate.

A SEM of the vertical diamond field emission triode is shown in Fig. 3. The fabricated diamond emitter has a very sharp apex (~5 nm), surrounded by a self-aligned silicon gate. The diamond cathode is electrically insulated from the silicon gate by a 2-μm-thick SiO<sub>2</sub> layer. Fig. 4 shows an SEM of a lateral diamond field emission diode with four diamond “fingers” configured as a field emission cathode and a diamond anode located 2 μm laterally away from the diamond fingertips.

### 3. Field emission results and discussion

The fabricated diamond emission diodes and triodes were tested for electron emission under vacuum at 10<sup>-6</sup> torr. The emission current was recorded as a function of applied voltages. Fowler–Nordheim (F–N) equation was used to analyze the diamond field emission data

$$\ln(I/E^2) = \ln(A \cdot K_1 \cdot \beta^2 / \Phi) - (K_2 \cdot \Phi^{1.5} / \beta)(1/E) \quad (1)$$

where  $K_1$  and  $K_2$  are constants:  $K_1 = 1.54 \times 10^{-6}$  AeV/V<sup>2</sup>,  $K_2 = 6.83 \times 10^7$  V/(cm eV<sup>3/2</sup>),  $I$  is the emission current,  $\Phi$  is the work function of the emitting surface in eV,  $\beta$  is the geometrical field enhancement factor,  $A$  is the emitting area and  $E$  is the applied electric field.

Fig. 5 shows the field emission behavior of a vertical diamond field emission diode while inset shows the corresponding F–N plot. The data was plotted using a special anode assembly called the indented anode as shown in Fig. 6 for reasons specified later. The turn-on field was ~15 V/μm. A high emission current of over 0.1 A (using pulse mode of 30 s duration) was recorded at 1670 V (34 V/μm). The linear F–N plot in the inset of Fig. 5 demonstrates the emission current of the diamond diode conforms to F–N behavior. The F–N plot shows two straight lines with different slopes. The line with the lower slope corresponds to low emission current regime (low emission field) and one with steeper slope corresponds to the high emission current region (high emission field). One explanation of the observed behavior could be: at lower electric field, emission occurs only from the sharper tips in the array. This leads to a smaller emission area (i.e. smaller extrapolated y-intercept value per the F–N equation) with very high field enhance-

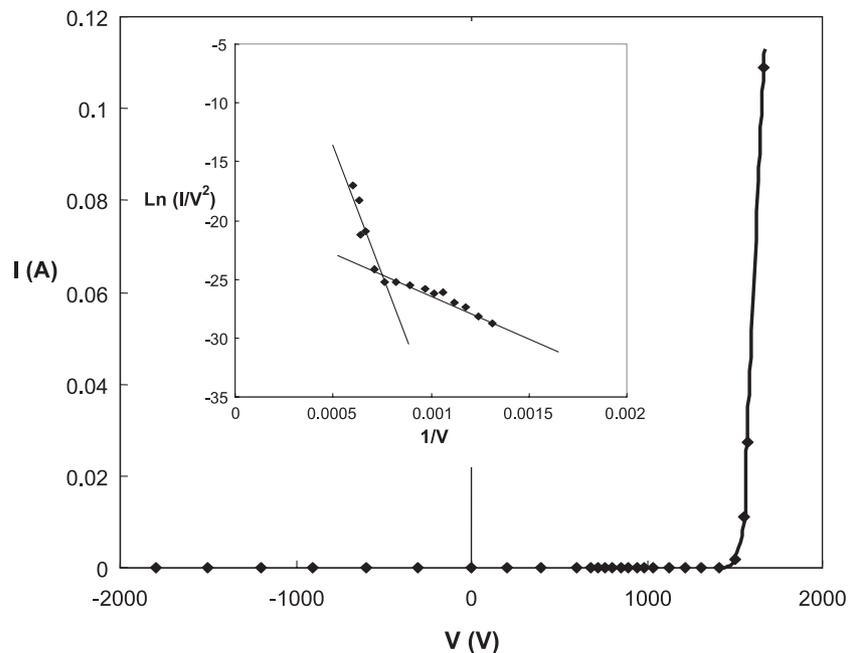


Fig. 5.  $I$ – $V$  plot of diamond vacuum diode with high emission current. Inset shows the corresponding F–N plot.

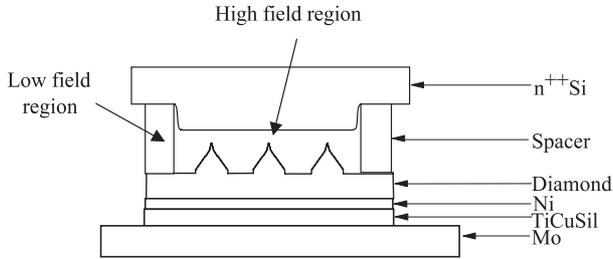


Fig. 6. Diode test configuration with indented anode.

ment factor  $\beta$ , leading to the observed lower current but a shallow F–N slope. At higher electric fields, more tips (including the less sharper tips) in the array are able to emit with an effective overall lower  $\beta$ . This leads to a higher emission area (i.e. bigger extrapolated  $y$ -intercept value per the F–N equation) with lower field enhancement factor and hence the observed high current but a steeper F–N slope. The high current measured conforms to F–N field emission theory and differs from gas discharge phenomenon. The high emission current capability of this diamond vacuum diode is attributed to the ability to produce diamond emitters in array configuration by the molding method, the indented anode design and the high thermal conductivity of diamond. The indented-edge anode was designed so as to allow the use of a thicker spacer to withstand high voltage and at the same time have smaller anode–cathode spacing than the spacer [6]. Using this special indented anode design, a vertical diamond field emission diode operable at high current is demonstrated.

The electron emission characteristics, anode emission current versus anode voltage ( $I_a$ – $V_a$  plots), of a self-aligned gated diamond triode for various gate voltages ( $V_g$ ) are shown in Fig. 7. The electrical characteristics of the diamond triode were characterized in a common emitter configuration. The plots demonstrate the linear and saturation behavior expected of a field-emission transistor. Saturation is seen for various gate voltages at anode voltage above 60 V. The figure indicates a low turn-on gate voltage of 22 V and a high emission current of 200  $\mu$ A at a gate voltage of 32 V for an anode voltage of 300 V. The triode shows a high DC gain of 800 as evident from the figure. The DC gain of a triode is defined as

$$\mu = \frac{dV_a}{dV_g}, \text{ at } I_a = \text{constant} \quad (2)$$

For which, the anode voltage  $V_a$  changes from 150 to 400 V, while the gate voltage  $V_g$  has to change from 31.7 to 31.4 V at a constant anode current  $I_a$  of 150  $\mu$ A. The AC characteristics of the field emission triode show a high AC voltage gain of  $\sim 65$  with a high output voltage of  $\sim 100$  V for an input voltage of  $\sim 1.5$  V as shown in Fig. 8. This indicates that the diamond field emission triode provides a high voltage gain when operated as an amplifier and is a very promising prospect for signal amplification applications.

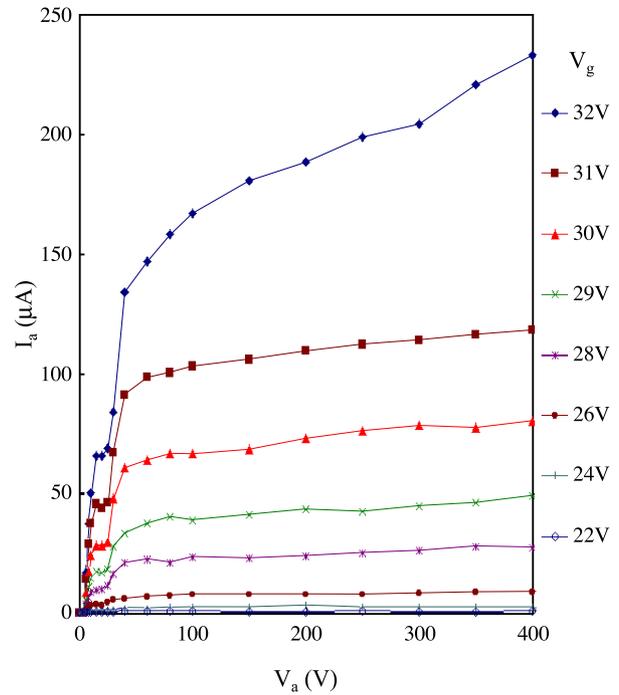


Fig. 7.  $I_a$ – $V_a$ – $V_g$  plot of self-aligned gated diamond triode.

The emission characteristic of a lateral diamond field emission diode is shown in Fig. 9. The figure shows that the lateral diamond field emitter has a very low turn-on voltage of  $\sim 5$  V and a high emission current of 6  $\mu$ A, from the four diamond fingers, at an anode voltage of 25 V. The anode–cathode spacing is  $\sim 2$   $\mu$ m. Thus, the lateral field emitter exhibits a very low turn-on field of  $\sim 3$  V/ $\mu$ m, which is the lowest value reported for lateral field emitters [7–9]. Inset of Fig. 9 shows the corresponding F–N plot for lateral field emitter. The linearity of this plot confirms the observed current to originate from electron field emission. The shallow slope ( $\sim 9$  V/ $\mu$ m) of the F–N plot implies that the lateral diamond emitter diode has a high field enhancement factor. This high field enhancement factor is due to the fact that the diamond finger cathodes are made up of very small grain geometries with the smallest grain size of  $\sim 5$ –10 nm as observed from high magnification SEM pictures. High field enhancement factor can also be attributed to the  $sp^2$  content of the film and presence of boron dopant in the diamond film [10]. It should be noted that boron-doped p-type

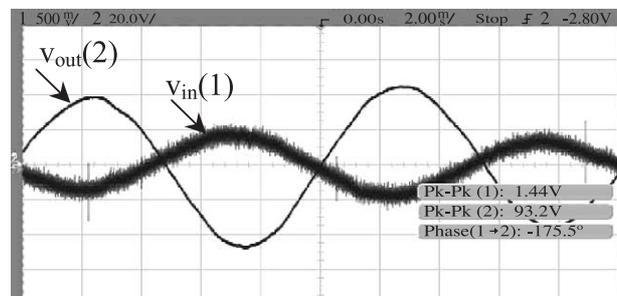


Fig. 8. AC characteristics of self aligned vacuum triode.

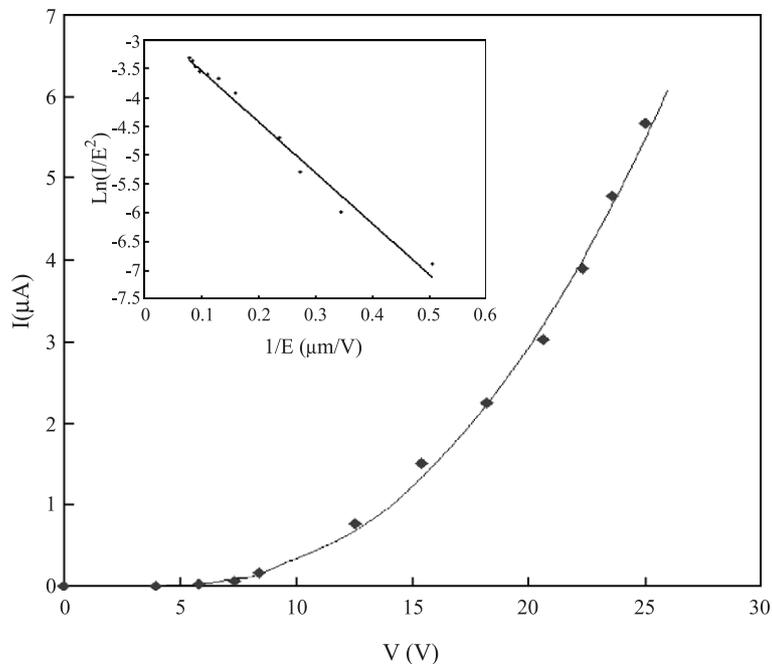


Fig. 9.  $I$ – $V$  plot of lateral diamond emitter diode. Inset shows the corresponding F–N plot.

diamond without the incorporation of  $sp^2$  content in the diamond film would degrade the field emission due to high work function [10–12]. However, it is clear that lateral diamond field emitters exhibit excellent field emission characteristics even prior to any application of special submicron photolithography patterning.

#### 4. Conclusion

In conclusion, a diamond field emission diode operable at high emission current over 0.1 A in an indented anode vertical configuration has been demonstrated. A diamond field emission triode with excellent transistor characteristics of high DC voltage gain and large AC voltage amplification is achieved. A lateral diamond field emitter with the lowest turn-on voltage and high emission current has been realized. Diamond vacuum emission diode with high emission current offers great promise in high current and high power applications, while diamond field emission triodes exhibiting comparable characteristics with solid state MOSFETs have promise for potential integrated circuit compatible vacuum microelectronic applications. An efficient lateral

diamond field emitter has potential applications in sensors and microelectromechanical systems.

#### References

- [1] J. van der Weide, Z. Zhang, P.K. Baumann, M.G. Wemmsell, J. Bernholc, R.J. Nemanich, *Phys. Rev.*, B 50 (1994) 5803.
- [2] I.L. Kravinsky, V.M. Asnin, G.T. Mearini, J.A. Dayton, *Phys. Rev.*, B 53 (1996) 7650.
- [3] I.L. Kravinsky, V.M. Asnin, *Appl. Phys. Lett.* 72 (1998) 2574.
- [4] M.W. Geis, J.C. Twichell, J. Macaulay, K. Okano, *Appl. Phys. Lett.* 67 (1995) 1328.
- [5] M.W. Geis, J. Gregory, B.B. Pate, *IEEE Trans. Electron Devices* 38 (1991) 619.
- [6] A. Wisitsora-at, W.P. Kang, J.L. Davidson, M. Howell, W. Hofmeister, D.V. Kerns, *J. Vac. Sci. Technol.*, B 21 (4) (2003).
- [7] C.S. Lee, J.D. Lee, C.H. Han, *IEEE Electron Device Lett.* 21 (2000) 479.
- [8] M.Y.A. Turner, R.J. Roedel, M.N. Kozicki, *J. Vac. Sci. Technol.*, B 17 (1999) 1561.
- [9] S.S. Park, D.I. Park, S.H. Hahm, J.H. Lee, H.C. Choi, J.H. Lee, *IEEE Trans. Electron Devices* 46 (1999) 1283.
- [10] A. Wisitsora-at, W.P. Kang, J.L. Davidson, Q. Li, J.F. Xu, D.V. Kerns, *Appl. Surf. Sci.* 146 (1999) 280.
- [11] C. Bandis, B.B. Pate, *Appl. Phys. Lett.* 69 (1996) 366.
- [12] R. Schlessler, et al., *Appl. Phys. Lett.* 70 (1997) 24.