Electronics Development
for pSec Time-of-Flight Detectors

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Introduction: **Readout Electronics System**

**Anode structure**

**Harold’s TOF system**
Characteristics of MCP-PMT Output Signal

MCP-PMT output signal from Tim’ simulation

- Rise time 15ps (equivalents to a signal bandwidth of 23.3 GHz)
- Pulse width (FWHM): 40ps
- Reflection coefficient: -0.98 (Load=100 ohms)
- Reflection time delay (round trip): 240ps
- Recovery time: 75ns (Settled at 1ppm)
Proposed Time Stretcher TDC with 1ps Resolution

Start

MCP_PMT Output Signal

Stop

500ps

Reference Clock

"fine" time interval

Tw

psFront-end

Comparator

I_2 \ll I_1
**Electronics Requirements & Process Evaluations**

**Input signal bandwidth:** ~23.3GHz  
**Input signal width (FWHM):** ~40ps  
**TDC resolution:** ~1ps

**Minimum Requirements:**
- ultra low noise, ultra high $f_T$ transistors  
  > 5-10x of the input signal bandwidth ~ (110-220GHz)  
- stable passive components  
  Inductors, MIM Capacitors, Resistors, Varactors ...

**Available Processes:**
- IHP SiGe BiCMOS 0.25μm technology:  
  (SG25H1, SG25H2) --- Europractice  
- IBM SiGe BiCMOS 0.13μm Technology:  
  (8HP) --- MOSIS
UC designed 2 GHz VCO with 55 fsec Cycle-to-Cycle Timing Jitter Using IHP SG25H1 Process
**Brief Summary of IBM BiCMOS8HP Process**

- **SiGe hetero-junction bipolar transistors**
  - $f_T$ (high performance): $200\text{GHz}$, $BV_{ceo}=1.7V$, $BV_{cbo}=5.9V$
  - $f_T$ (high breakdown): $57\text{GHz}$, $BV_{ceo}=3.55V$, $BV_{cbo}=12V$

- **High-Q inductors and metal-insulator-metal capacitors**

- **4 types of low-tolerance resistors with low and high sheet resistivity**
  - $n+$ diffusion, tantalum nitride, $p+$ polysilicon and $p-$ polysilicon

- **CMOS transistors (VDD=1.2V or 2.5/3.3V)**
  - Twin-well CMOS
  - Hyperabrupt junction and MOS varactors

- **Deep trench and shallow trench isolations**
8HP NPN Ft Characteristics vs. Emitter size (25C)
2GHz VCO Design using IBM SiGe BiCMOS8HP Process

EDA Tools:
Cadence Virtuoso
Analog Environment

Verification Tools:
Diva/Assura

Simplified VCO Schematic

- Purely hetero-junction transistors
- Negative resistance
- On-chip high-Q LC tank
- High Frequency PN diode Varactors
- Capacitor voltage dividers
- 130Mhz tuning range
- Full differential 50-ohm line drivers
VCO Schematic (Pre-layout) Simulation Result

Transit Outputs

Phase Noise

Phase Noise -97dBc/Hz
Equivalents to Cycle-to-cycle timing jitter of 5 fs

V-F Transfer Function

Tuning Range=130M
2GHz@VC=1.35V
Analysis of CMOS Latchup

Famous CMOS latch-up which created by parasitic lateral pnp and npn transistors

Solution: apply substrate contacts and tie them to the lowest voltage terminals
apply shallow trenches to increase isolation
Substrate Noise Minimization

(1) One of the major substrate noise is caused by current injection from bipolar transistors working in saturation mode.
(2) Substrate PN diode occasionally forward biased by EMI interference or some other reasons.
(3) Parasitic coupling capacitance

Solution:
Prevent transistors from working in saturation mode unless you have to.
apply substrate contacts and tie them to the lowest voltage potential on the chip.
apply deep or shallow trench shielding rings to increase isolation
UC Designed 2GHz VCO Chip with 5 fsec Cycle-to-Cycle Time Jitter
Using IBM 0.13μm SiGe BiCMOS8HP Process (Feb. 2007)

Chip Size: 850x640μ
Layout and Parasitic Extraction

- Diva/Assura DRC Check
- Diva/Assura LVS Check
- Floating Gate, NWell & Antenna Check
- Global Pattern Density Check
- Local Pattern Density Check
- GR594 (Dendrite Rules) Check
- Assura RCL extraction
- GDSII Stream Out (CDS → GDSII mapping)
- GDSII/Layout Comparison Check

Backup your full data after you passed all checks!!!
**Schematic & Post Layout Comparison:** *Hierarchy Setup*

**Schematic**

**av_Extracted (RCL)**
Node_Tn: 
\[ \Sigma C = 119.8f \]
\[ \Sigma L = 73p\text{H} \]
Post Simulation: Configuration Setup

Parasitic Parameters

Back Annotation
### Post Simulation Parasitic Parameter List

<table>
<thead>
<tr>
<th>Instance</th>
<th>Inherited View List</th>
</tr>
</thead>
<tbody>
<tr>
<td>c3850 (analogLib pcapacitor spectre)</td>
<td>spectre cmos_sch cmos.sch ...</td>
</tr>
<tr>
<td>c3851 (analogLib pcapacitor spectre)</td>
<td>spectre cmos_sch cmos.sch ...</td>
</tr>
<tr>
<td>c3852 (analogLib pcapacitor spectre)</td>
<td>spectre cmos_sch cmos.sch ...</td>
</tr>
<tr>
<td>c3853 (analogLib pcapacitor spectre)</td>
<td>spectre cmos_sch cmos.sch ...</td>
</tr>
<tr>
<td>c3854 (analogLib pcapacitor spectre)</td>
<td>spectre cmos_sch cmos.sch ...</td>
</tr>
<tr>
<td>c3855 (analogLib pcapacitor spectre)</td>
<td>spectre cmos_sch cmos.sch ...</td>
</tr>
<tr>
<td>c3856 (analogLib pcapacitor spectre)</td>
<td>spectre cmos_sch cmos.sch ...</td>
</tr>
<tr>
<td>c3857 (analogLib pcapacitor spectre)</td>
<td>spectre cmos_sch cmos.sch ...</td>
</tr>
<tr>
<td>c3858 (analogLib pcapacitor spectre)</td>
<td>spectre cmos_sch cmos.sch ...</td>
</tr>
<tr>
<td>c3859 (analogLib pcapacitor spectre)</td>
<td>spectre cmos_sch cmos.sch ...</td>
</tr>
<tr>
<td>c3860 (analogLib pcapacitor spectre)</td>
<td>spectre cmos_sch cmos.sch ...</td>
</tr>
<tr>
<td>c3861 (analogLib pcapacitor spectre)</td>
<td>spectre cmos_sch cmos.sch ...</td>
</tr>
<tr>
<td>c3862 (analogLib pcapacitor spectre)</td>
<td>spectre cmos_sch cmos.sch ...</td>
</tr>
<tr>
<td>c3863 (analogLib pcapacitor spectre)</td>
<td>spectre cmos_sch cmos.sch ...</td>
</tr>
<tr>
<td>l1.1 (analogLib pcapacitor spectre)</td>
<td>spectre cmos_sch cmos.sch ...</td>
</tr>
<tr>
<td>l1.2 (analogLib pcapacitor spectre)</td>
<td>spectre cmos_sch cmos.sch ...</td>
</tr>
<tr>
<td>l1.3 (analogLib pcapacitor spectre)</td>
<td>spectre cmos_sch cmos.sch ...</td>
</tr>
</tbody>
</table>

#### Tree View

- **Instance**: `c3850` (analogLib pcapacitor spectre)
- **Inherited View List**: spectre cmos_sch cmos.sch ...

- **Instance**: `l1.1` (analogLib pcapacitor spectre)
- **Inherited View List**: spectre cmos_sch cmos.sch ...

- **Instance**: `l1.2` (analogLib pcapacitor spectre)
- **Inherited View List**: spectre cmos_sch cmos.sch ...

- **Instance**: `l1.3` (analogLib pcapacitor spectre)
- **Inherited View List**: spectre cmos_sch cmos.sch ...

- **Instance**: `rg_1.307` (analogLib presistor spectre)
- **Inherited View List**: spectre cmos_sch cmos.sch ...

- **Instance**: `rg_1.308` (analogLib presistor spectre)
- **Inherited View List**: spectre cmos_sch cmos.sch ...

- **Instance**: `rg_1.309` (analogLib presistor spectre)
- **Inherited View List**: spectre cmos_sch cmos.sch ...

- **Instance**: `rg_1.310` (analogLib presistor spectre)
- **Inherited View List**: spectre cmos_sch cmos.sch ...

- **Instance**: `rg_1.311` (analogLib presistor spectre)
- **Inherited View List**: spectre cmos_sch cmos.sch ...

- **Instance**: `rg_1.312` (analogLib presistor spectre)
- **Inherited View List**: spectre cmos_sch cmos.sch ...

- **Instance**: `rg_1.315` (analogLib presistor spectre)
- **Inherited View List**: spectre cmos_sch cmos.sch ...

- **Instance**: `rg_1.319` (analogLib presistor spectre)
- **Inherited View List**: spectre cmos_sch cmos.sch ...

- **Instance**: `rg_1.322` (analogLib presistor spectre)
- **Inherited View List**: spectre cmos_sch cmos.sch ...

- **Instance**: `rg_1.326` (analogLib presistor spectre)
- **Inherited View List**: spectre cmos_sch cmos.sch ...

- **Instance**: `rg_1.358` (analogLib presistor spectre)
- **Inherited View List**: spectre cmos_sch cmos.sch ...

- **Instance**: `rg_1.424` (analogLib presistor spectre)
- **Inherited View List**: spectre cmos_sch cmos.sch ...

- **Instance**: `rg_1.425` (analogLib presistor spectre)
- **Inherited View List**: spectre cmos_sch cmos.sch ...

- **Instance**: `rg_1.434` (analogLib presistor spectre)
- **Inherited View List**: spectre cmos_sch cmos.sch ...
Schematic/Post Layout Simulation Comparison:
Transit Outputs (first layout)

V_{\text{max}} = 1.52 \text{V} (Schematic, Transit Outputs)

V_{\text{max}} = 1.475 \text{V} (Layout Extraction, Transit Outputs)
VCO Post Layout Simulation Result (First Layout)

Output Phase Noise Spectra Plot

psdesign 2gvcoc208 av_extracted : Feb 14 16:41:16 2007

Phase Noise; dBC/Hz, Relative Harmonic = 1

Periodic Noise Response

\[ M_0(-97.53 \text{ dBC/Hz}) \]

relative frequency (Hz)
Schematic/Post Layout Simulation Comparison:

V-F Transfer Function Plot (first layout)

- Designed Schematic V-F Transfer Function
  - Frequency = 2Ghz @ VC = 1.35V
  - Tuning Range = 130MHz

- Post-layout V-F Transfer Function
  - Frequency = 2Ghz @ VC = 0.9V
  - Tuning Range = 80MHz
VCO Post Layout Transit Simulation Result (Final)

Transit Output Waveforms

Modify schematic design
Re-layout
Re-simulation
VCO Post Layout Simulation Result (Final)

Output Phase Noise Spectra Plot

Phase Noise: $\text{dBc/Hz}$, Relative Harmonic = 1

Periodic Noise Response

Equivalents to RMS cycle-to-cycle time jitter of 5 femto-seconds

$$J_c^2 = \frac{f_{os}^2 \mathcal{L}(f)}{f_c^3}$$

$0(-97.19 \text{dBc/Hz})$
VCO Simulation Result (Final)

V-F Transfer Function Plot

Schematic V-F Transfer Function

Post Layout V-F Transfer Function
F=2GHz@VC=1.35V
Tuning Range=130MHz
Conclusion

(1) IBM 0.13\(\mu\)m SiGe BiCMOS8HP has been evaluated; it is a user-friendly design kit.

(2) Circuit performance meets our requirements (very) well.

(3) MOSIS has resumed 8HP Multi-Project Wafer runs – schedule has been changing(!). We are in the process of understanding how to proceed toward a full chip design starting with our first little VCO chip.

(4) Challenging Issues for the entire readout electronics.

Thanks!