INTRODUCTION

In the context of picosecond timing, analog detector pulse sampling in the 10 pico-second range starting from a signal pedestal until its decay after the peaking, provides information to get accurately:

- The instant of the first electrons arrival
- The pulse amplitude

In practice, a deep-submicron CMOS based Vernier timing generator locked on a 500 MHz clock, for instance, [1] can provide, for instance, 10-20 ps spaced controls to 100-200 analog storage elements (of the order of few hundreds fF capacitors each) for a total duration of a few ns, long enough to get efficiently pedestal, rising edge, and the peaking value of any pulse to be acquired. This timing generator can fuel several independent channels.

More precisely, the sampling process would run continuously as a circular analog buffer, stopped on receipt of a response from a triggering discriminator after a delay allowing to store several samples of the pedestal before the triggering instant. This triggering device does not need to be extremely fast, since the samples will be time stamped using the main clock and Vernier timer. The main clock and trigger response can be acquired on two separate (but identical) sampling channels for calibration and monitoring purposes.

Therefore, a multi-channel 50-100 GHz sampling device does not seem out of reach using deep-submicron CMOS integrated technologies. A block diagram is shown Figure 1.

I ANALOG SAMPLING

Analog sampling in the 10 picoseconds range allows to reconstruct both time and amplitude, using for instance W. E. Cleland and E.G. Stern algorithm [2]. Another method to derive the first electrons arrival time is to fit the rising edge using polynomials or splines, and intersect the pulse baseline with the fit extrapolated. Simulations are under progress in order to determine the best technique, for a given pulse shape and noise. Preliminary Monte-Carlo performed with synthesized signals from Micro-Channel Plates detectors amplifying 50 photo-electrons with 10 μm pores show that the picosecond range precision can be obtained using the rising edge fit method, using a sampling rate of 20 GHz.

Main parameters for the sampling process are:

- Sampling frequency
- Number of points
- Sampling start and duration wrt pulse shape
- Sampling accuracy
- Acceptable droop
II IMPLEMENTATION

II-1 IC Technologies

The mixed CMOS deep sub-micron technologies (130-90nm) are well-suited to a fast implementation. The availability of several kinds of MOS transistors (high speed, low $V_t$, zero $V_t$, low leakage) transistors together with Metal-Insulator-Metal capacitors (MiM) allows to implement efficient differential storage devices with accurate read and write capability.
II-2 Architecture

- Timing generator

Gate propagation delays of the order of tens of pico-seconds used as delay elements locked on an external reference clock running around 500 MHz. A Vernier technique such as successfully implemented in the HPTDC chip [1] should derive 20-30 ps equally spaced time references over one clock period, with the use, for instance, of starved inverters [3] as voltage controlled delay elements.

The technological spreads of these delays has been measured to less than one pico-second [4] in both 130 and 90nm CMOS technologies. This low spread will ensure a reproducible and reliable performance for such a timing generator. Locked on the 500 MHz clock, a main Delay Locked Loop (DLL) of eight elements provides $2 \text{ ns} / 8 = 125 \text{ ps}$ equally spaced references. Eight secondary delay lines phase locked on each tap of the main DLL, comprising nine elements, for instance, would provide $9 \times 8 = 72$ references with time steps of $(2\text{ns} / 9 - 2\text{ns} / 8) = 28 \text{ ps}$ as shown on Figure 2. It is clear that the layout of this DLL array is one of the most, if not the most critical task. Estimations of cross talk should result from post-layout simulations.

![Figure 2. Vernier timing generator](image-url)
- Analog storage

A bank of MiM capacitors of, for instance, 250 fF values (area of 12 x 12 =144 μm²) Therefore, taking into account the area for the associated switches, a total area of 500 μm² per cell could be foreseen, in a 130 nm CMOS technology, even less in 90 nm. A differential implementation would be preferred, feeding the storage capacitance with symmetric signals.

- Triggering discriminators

The input signals are sampled continuously. Whenever an input level exceeds a given (programmable) threshold, the corresponding channel is stopped after a (programmable) delay. This delay allows to record part of the trailing edge of the pulse. To take into account the walk (slope dependent) spreads of the discriminator, a sufficient sampling duration should be foreseen.

- Analog to Digital conversion

The optional output AD converter digitizes the sampler outputs containing relevant data (i.e. those whose triggering discriminator stopped the recording process). An analog multiplexer allows to select the proper channels and analog memory cells. A 10-bit Wilkinson looks the most efficient architecture for that particular task where a high level of parallelism is required. A Wilkinson AD converter running 10 bits at 1 GHz (500 MHz clock, two edges) would convert 64 samples in 2¹⁰ x 1 ns = 1.024 μs which is faster compared to any successive approximation or pipeline AD converter. In addition, one single calibration is required.

- Control logic

The control logic generates the Write and Read controls for the analog sampler, includes control and status registers, Analog to Digital conversion control, I/O management and test modes.

II-3 Interfaces

An I/O list draft is sketched Table 1.

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<thead>
<tr>
<th>Pad name</th>
<th>Size</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inputs</td>
<td>128</td>
<td>Analog diff.</td>
</tr>
<tr>
<td>Outputs</td>
<td>16</td>
<td>LVDS</td>
</tr>
<tr>
<td>Clocks</td>
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<td>LVDS</td>
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<td>Vdd</td>
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<td>Gnd</td>
<td>70</td>
<td></td>
</tr>
<tr>
<td>Total</td>
<td>242</td>
<td></td>
</tr>
</tbody>
</table>

Table 1. I/Os
II-4 Silicon area

A 64-channel analog storage would occupy a Silicon area of 64 channels x 72 cells x 500 μm² = 2mm². Adding 20% for the discriminators, timing generator and control logic would result in a 2.4 mm² core chip. Two rows of I/O pads on four sides would result in a 2.25 x 2.25 = 5 mm² chip, including I/Os. The chip area is therefore bond pad dictated, unless a higher number of channels is integrated, if power allows.

II-5 Power

Charge storing power dissipates:
64 channels x 400 fF x 0.5V x 0.5V x 1/28 ps = 228 mW.
Other contributions from free running digital activity and low noise input sensing stages have to be evaluated.

REFERENCES


[3] S. Kleinfelder,
