Chicago Hawaii ASIC, Multi-Purpose [CHAMP] Overview:
Hawaii Designs

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On behalf of:
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Outline

- Background
- Hawaii Designs:
  - CSA
  - DAC
  - 2nd State Storage Array
  - D Flip-Flop
  - Voltage Controlled Delay Line
  - Waveform sampler
  - LVDS receiver
- Future

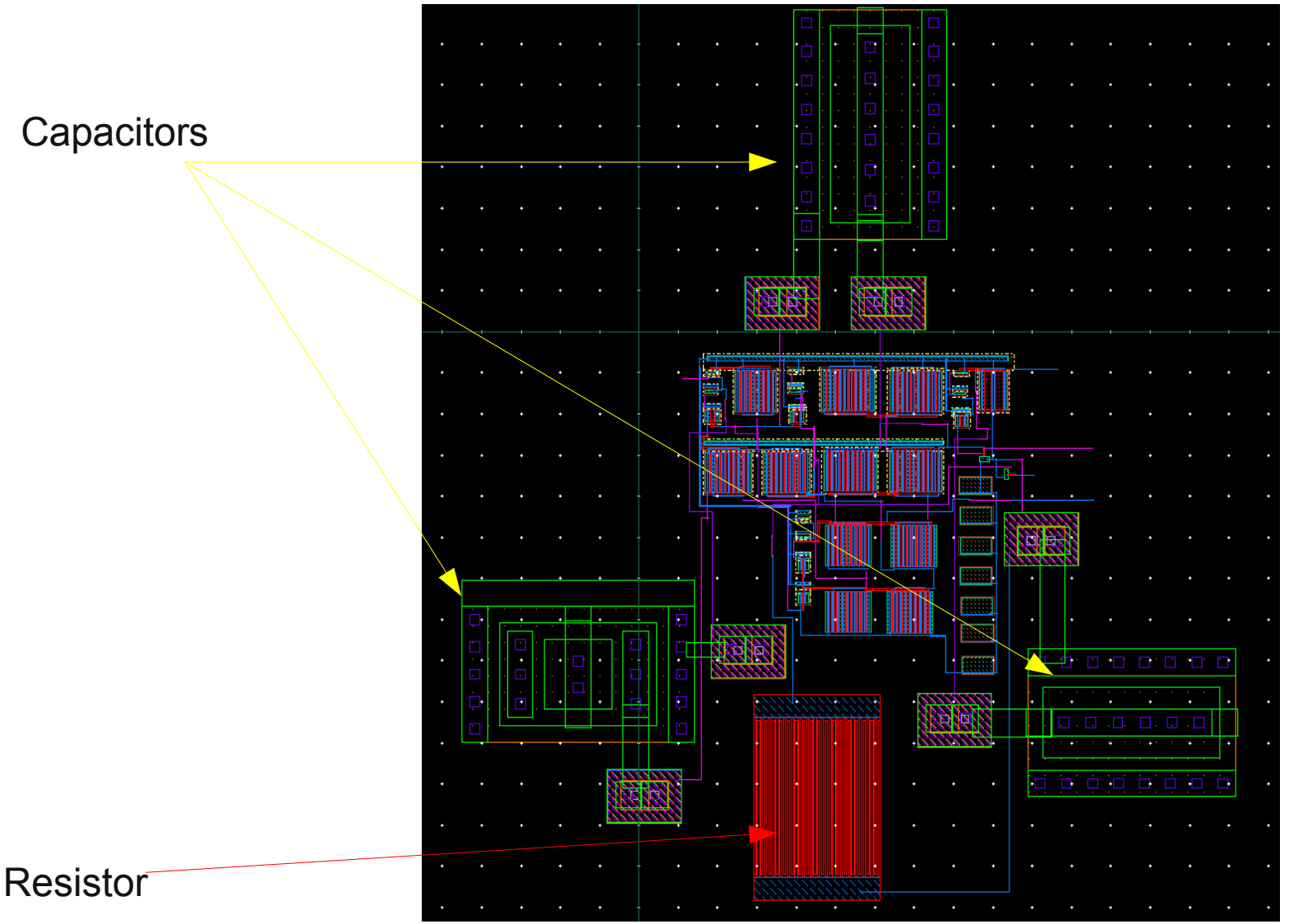
Background

- CHAMP ASIC
  - Joint U of Chicago and U of Hawaii test structure submission
  - Lays groundwork for future submissions
- Process: IBM 130nm
- First time in Hawaii using IBM process
- First ASIC design experience for:
  - Larry, Matt, Kurtis, Wei

Charge Sensitive Amplifier (CSA)

- Designed by Wei Cai
- Design goals:
  - 4ns rise time
- Overall dimensions:
  - 100μm wide by 112μm tall

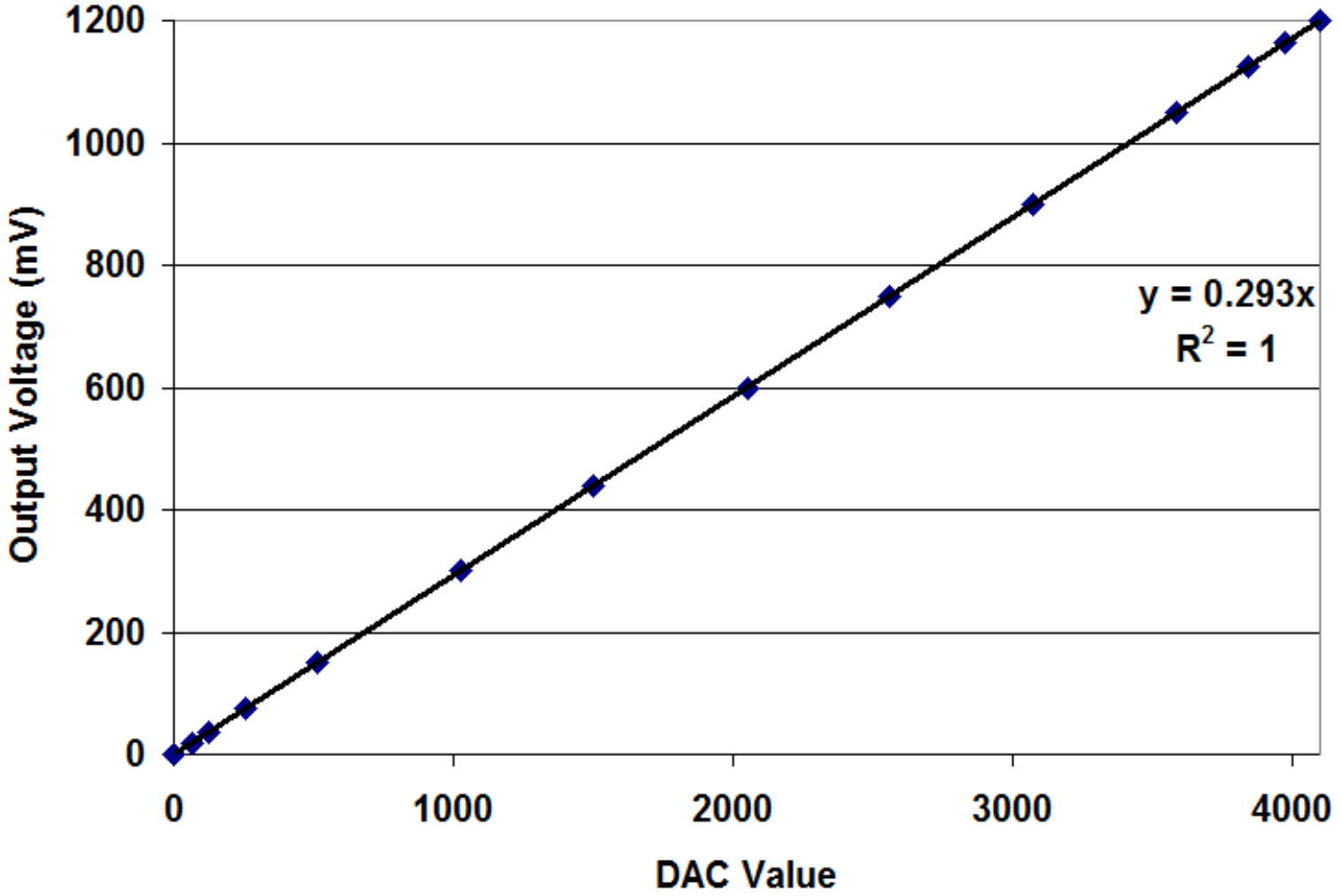
CSA: Layout



DAC

- Designed by Larry Ruckman
- Digital to Analog Converter:
  - R/2R design with SPI Interface
  - 12 bit resolution
  - 129.07 um by 51.23 um
  - Uses 1176 transistors
  - 6 external pins

DAC: 12 Bit Simulation

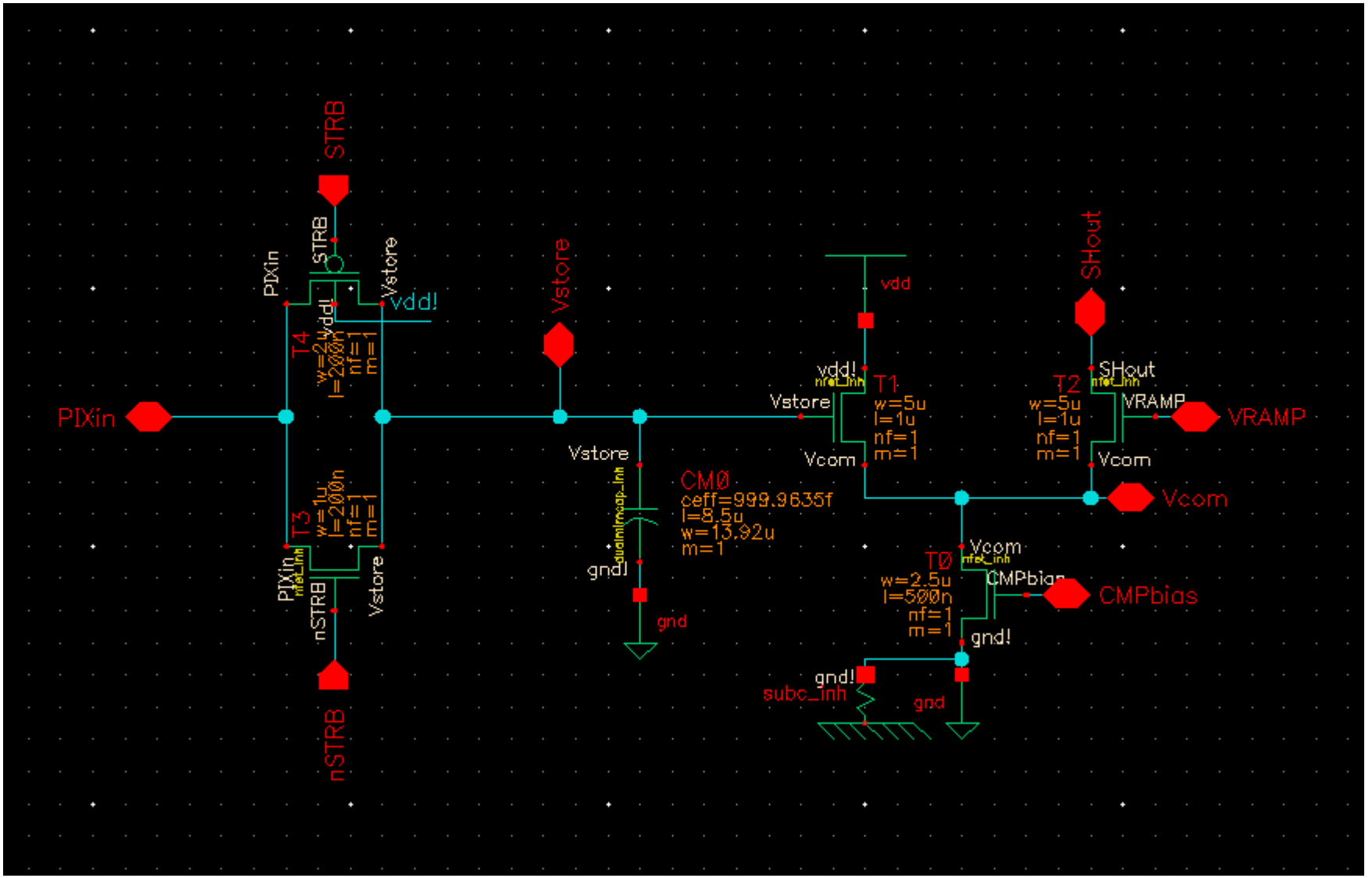


- LSB = (1.2 V)/(2^12) = 293 mV/count
- Theoretical slope agrees with simulation
- Slope errors in measurement will come from fabrication tolerances/errors

2nd Stage Storage Array

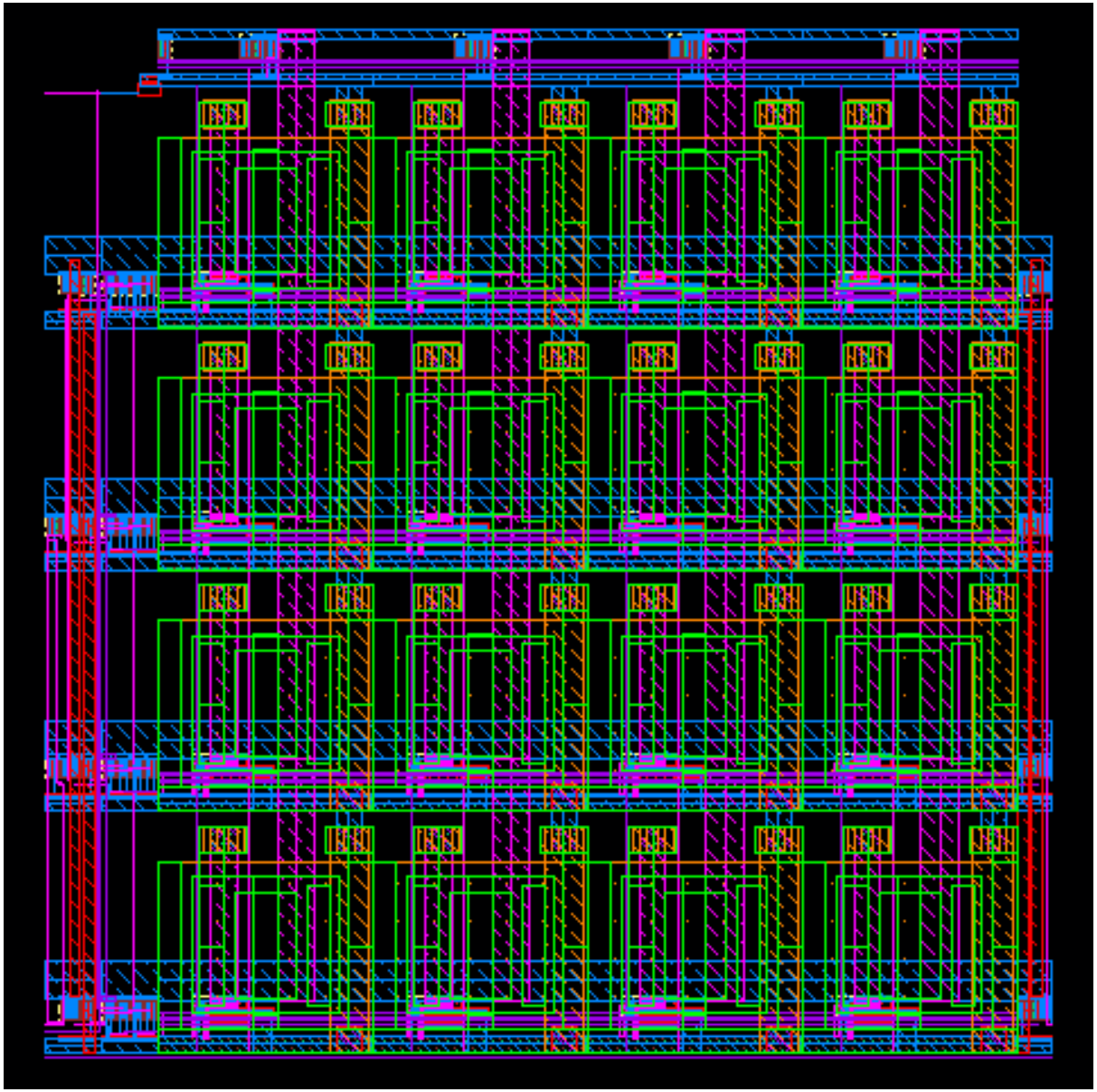
- Designed by Larry Ruckman
- Designed to perform long term storage (~ms) while avoiding large leakage currents as a second stage Wilkinson storage array.
- Uses large storage capacitors (1pF) with a differential pair.

Storage Array: Schematic



Storage Array: Layout

- 138.11 um by 135.33 um
- Includes address decoding, 16 cells
- Possibly a solution for deep storage in a future waveform ASIC designs in this process



D Flip Flop

- Designed by Matt Andrew
- Two designs:
  - NOR gates:
    - Simulates operation at 2.15GHz
    - Possibly up to 2.5GHz operation
  - NOR + NAND gates:
    - Simulates operation at 3.5GHz
    - 40μm by 26μm

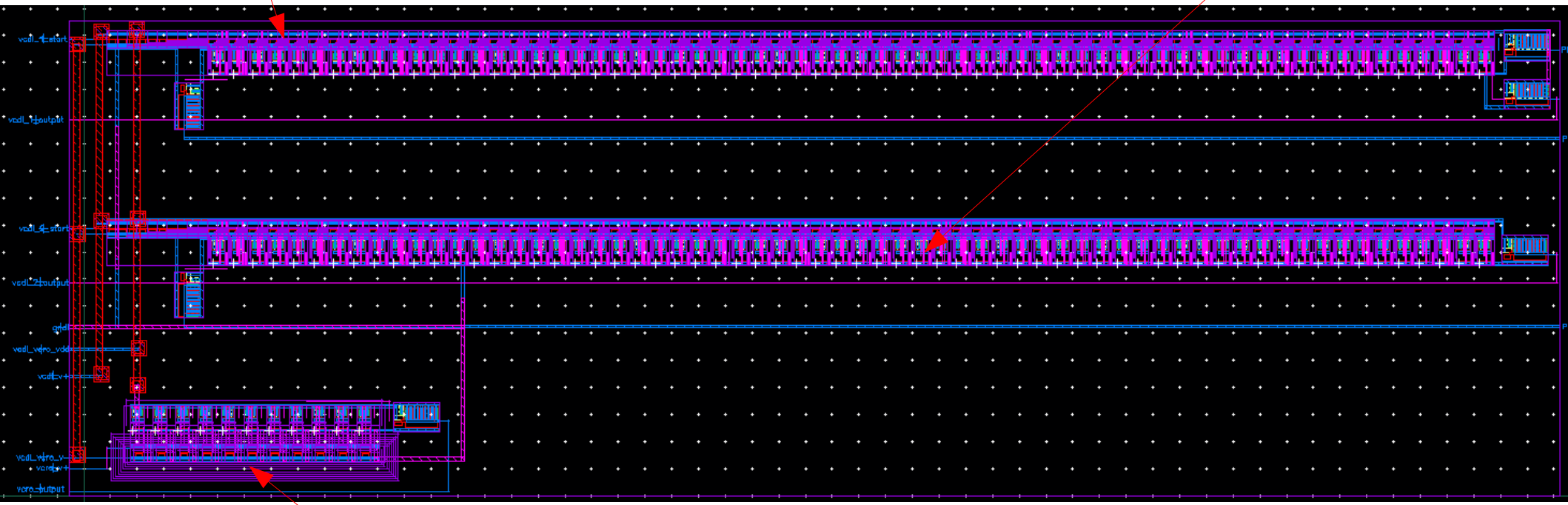
Voltage Controlled Delay Lines

- Designed by Matt Andrew
- Two delay lines
  - 64 stages with 9 stage delay
    - One delay line uses normal voltage FETs
    - One delay line uses low voltage FETs
- One ring oscillator
  - 11 stages with 9 stage delay
  - Several GHz in simulation (parasitics)

VCDL: Layout

Normal Vth VCDL

Low Vth VCDL



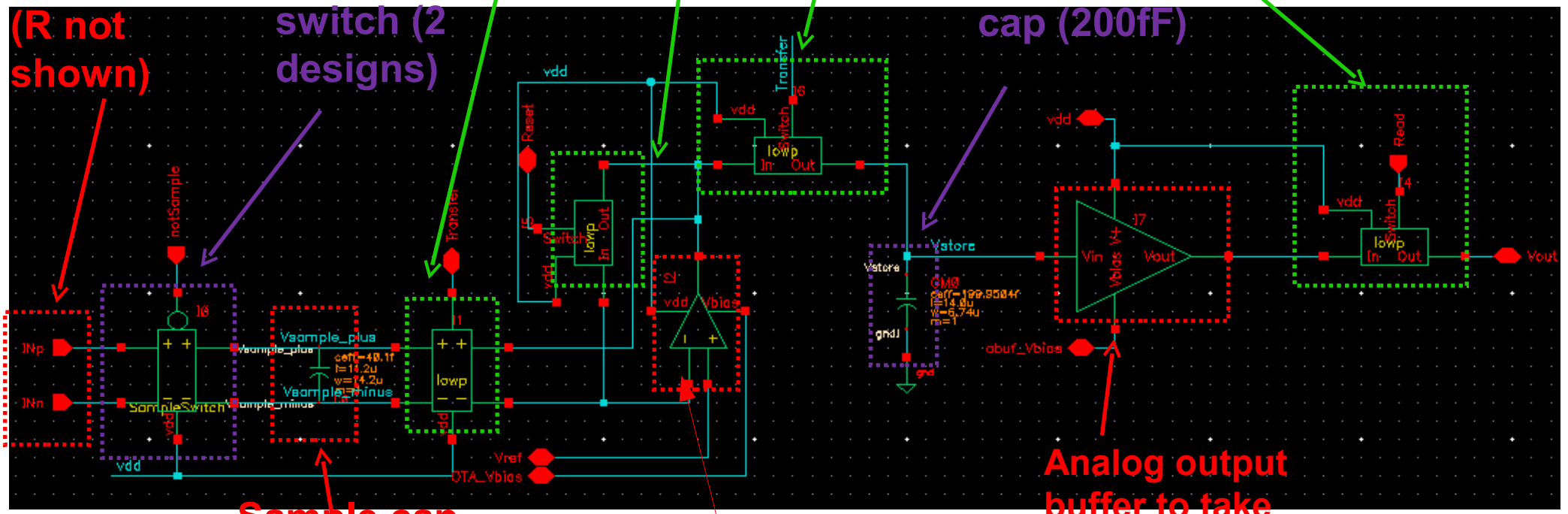
Ring oscillator

Waveform Sampling Arrays

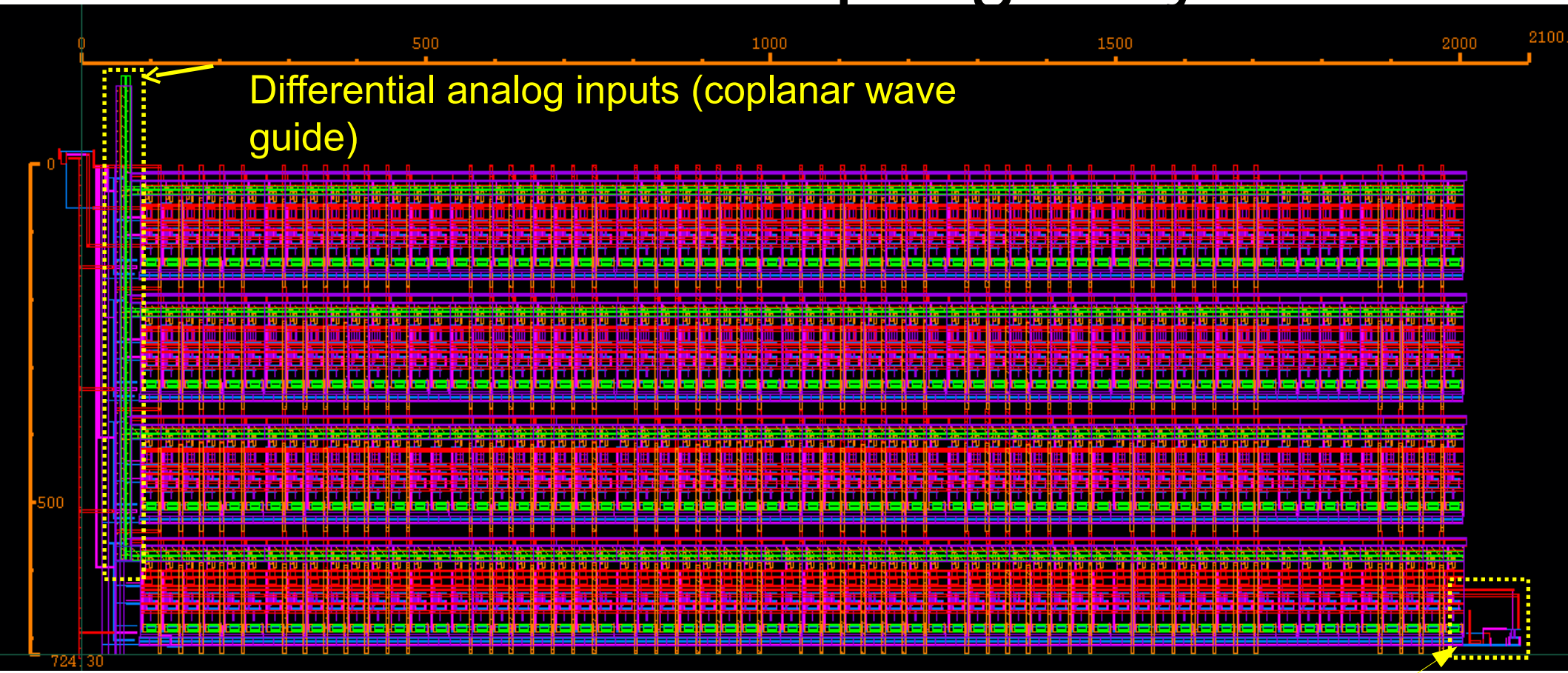
Four sampling arrays to explore high analog bandwidth sampling, compare simulated / measured bandwidth.

Simulated bandwidths (approximate): **1.8, 2.2, 2.6, 4.2 GHz**

Each sampling cell consists of 64 of the following basic cell:



Waveform Sampling: Layout



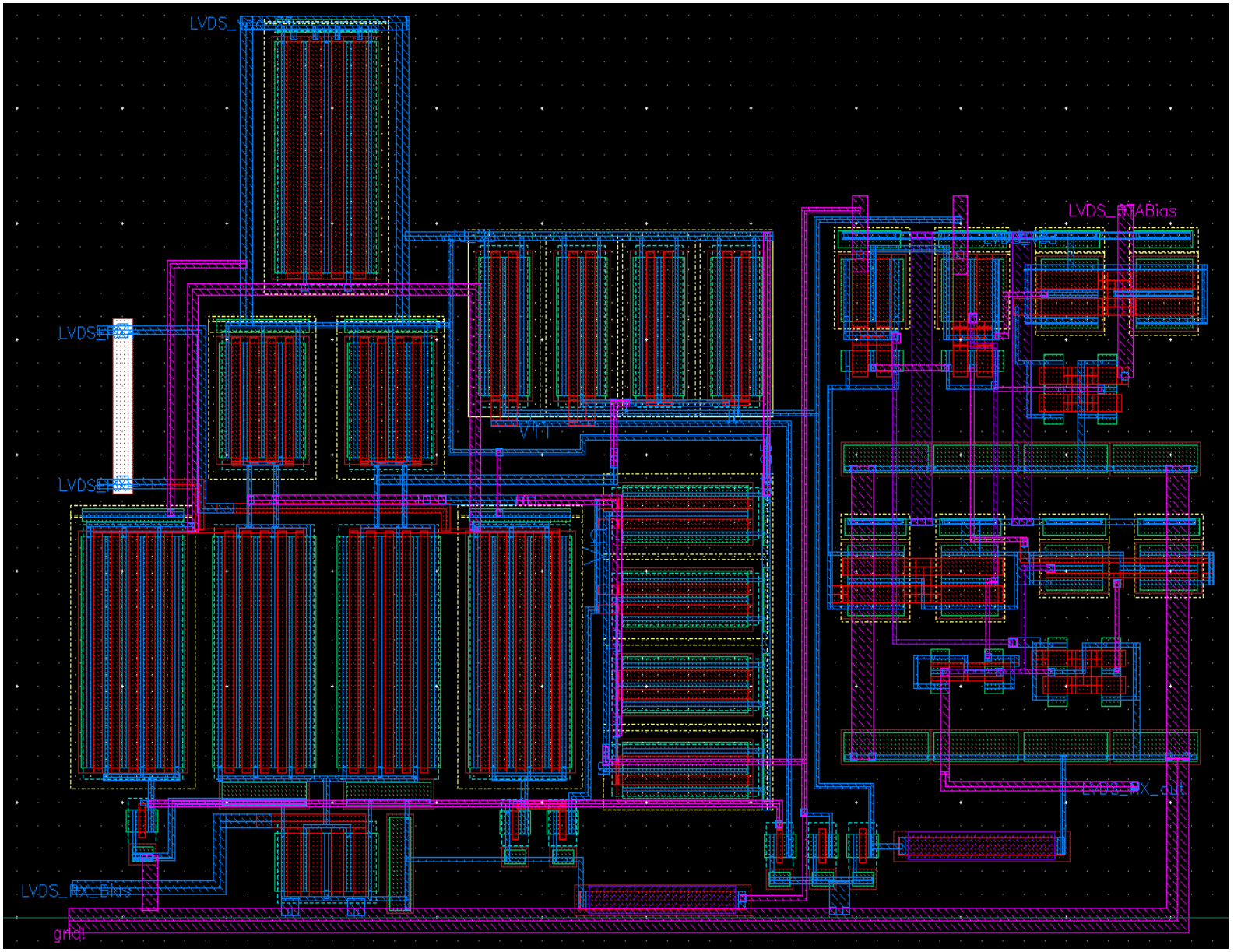
For each array:
- Delay line sits above to generate sampling
- Shift register sits below to control the read signals.
- Enable logic allows each array to be turned off/on for independent testing.

Independent test structures:
- OTA
- Analog output buffer

LVDS Receiver

- Designed by Mike Cooney
- A Low Voltage Differential Receiver
  - Translates 2.5V I/O to core 1.2V
  - Simulates operation at 1+ GHz
  - 100mV signal differential
  - 57μm wide by 47μm tall

LVDS Receiver: Layout



Conclusion

- May submission in IBM 130nm lays groundwork for future designs
  - High speed serial I/O interfaces (LVDS)
  - Deep sampling capability
  - Trim DACs for bias control
- First ASIC design experience for 4/5 Hawaii users