MCP Signal Extraction and Timing Studies

Kurtis Nishimura University of Hawaii LAPPD Collaboration Meeting June 11, 2010

Outline

- Studying algorithms to process pulses from MCP devices.
 - With the goal of finding an implementation that can be done quickly for on-line feature extraction with DSPs (as mentioned by Matt).
- Studies with:
 - Burle/Photonis Planacon (10 μ m pore)
 - Timing w/ CFDs versus waveform sampling algorithms.
 - Hamamatsu SL10 (10 μ m pore)
 - Software studies using high bandwidth oscilloscope data.

April 12, 2010 High resolution photon timing with MCP-PMTs: a comparison of commercial constant fraction discriminator (CFD) with ASIC-based waveform digitizers TARGET and WaveCatcher.

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*To be submitted to NIM A

Comparison btw Ortec CFD/TAC/ADC, and waveform digitizers (TARGET & WaveCatcher)

(1 GHz bandwidth)

Burle / Photonis Planacon with 10 μ m pore



N_{pe} ~ 30-50 for these tests.

| Parameter | Target | Wave |
|----------------------------------|-----------------|-------------------|
| | - | Catcher |
| Number of channels | 16 | 2 |
| Resolution | 9 bits | 12 bits(board) |
| | | >12.5 bits (chip) |
| Conversion time | <500 🗆 s/32 | 100 ns/one |
| | samples | sample |
| Termination | 90 Ω, 1kΩ, | >50 Ω (board) |
| | 10kΩ | > 1 MΩ (chip) |
| Power consumption | <10 mW/ch. | <2.5 W (board) |
| _ | | <300 mW(chip) |
| Sampling rate | 1-2.5 GSa/s | 0.4 to 3.2 GSa/s |
| Sampling bin in this test | ~450 ps/bin | 312.5 ps/bin |
| S/N ratio in this test * | ~50-60 | ~450 |
| Chip's front end BW in this test | ~150 MHz | 500 MHz |
| Storage depth (samples/channel) | 4096. | 256 |
| Trigger rates | Up to 50 kHz | Up to 30 kHz |
| Encoding | Wilkinson | On board ADC |
| Cross-talk to nearest channel | ~10% ** | <0.5% |
| Readout time (ASIC->FPGA) | 16 µs for 48/64 | ~30 µs for 256 |
| | cells over 16 | cells over the |
| | channels | two channels |
| External interface | USB 2.0 | USB 2.0 |

SLAC-PUB-14048

CFD Test Conditions

- a) Fermilab test beam (120 GeV/c proton)
- b) Laser test setup
- c) Electronics calibration setup



Test beam data raw (left) and time walk corrected (right). Laser results comparable.

ASIC Test Conditions



Analysis is performed with two algorithms:

Constant fraction algorithm

Simple software implementation of a constant-fraction discriminator.

- 1) Find peak voltage.
- 2) Find the time to cross a fraction of the peak voltage.

χ^2 algorithm

0.4

0.4

 Take many waveforms to determine an average pulse profile

2000 3000

2) Scan the profile over varying delays until you find the lowest $\chi^{\rm 2}$

Constant Fraction Algorithm

- Relatively simple, but still some knobs to tune...
 - Between waveform points, is it better to use linear interpolation or something else (e.g., spline).
 - Which fraction optimizes timing resolution?



$\chi^{\rm 2}$ Algorithm

- More complicated...
 - Same interpolation questions as CFD algorithm.
 - How much (and what section) of the waveform should be included in the χ^2 ?
 - →Generally best results were obtained with a polynomial fit to the first part of the leading edge.



χ^2 Algorithm

- How much (and what section) of the waveform should be included in the $\chi^{\rm 2}{\rm ?}$
 - Generally best results were obtained with a polynomial fit to the first part of the leading edge.



Timing Comparisons



→ Overall, results using χ^2 fitting are slightly better than those using a constant fraction algorithm, though there is significant added complexity.

→ Results with ASICs are competitive with hardware CFD as long as the analog bandwidth is high enough.

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Analysis of Fast PMT Pulses (Single γ)

- Timing studies also performed using the Hamamatsu SL10 w/ high bandwidth oscilloscope.
- Setup:

Gain (dB)



TDC Distributions (Single Photon Timing)



- Nagoya & Hawai'i measurement agree with each other
- Hawai'i has less of a tail in distribution
 - Less overall TDC RMS

Updated Analysis

- Previous analysis used waveforms "as-is" from the scope.
- What happens if we have lower bandwidth and/or a lower sampling rate.
 - To test, for example, expected performance from a waveform digitizing ASIC.
- New analysis steps:
 - 1. Take FFT of the raw scope waveform
 - 2. Apply low pass filter with varying 3dB points to simulate bandwidth limitations.
 - In this analysis, we use a 4th order Butterworth filter, but we can explore others, for example simulated frequency response of a waveform digitizing ASIC.
 - 3. Transform back to the time domain
 - 4. Downsample to simulate lower sampling rate.
 - We take every Nth point, with initial offset randomly chosen from 0 to N-1. We can make this more sophisticated as well, but interesting to start.
 - 5. Perform timing measurement similar to before.
 - We find the time to reach 30% of the measured peak voltage.

Sample Spectra, Waveforms









Conclusions

- Study is ongoing of various techniques for processing sampled waveform data, with focus on:
 - Simplicity / speed (as it needs to be done with on-line processing for many applications)
 - Performance (mainly in timing)
- So far, software CFD seems quite competitive with more complicated techniques.
- For future ASIC designs, it would be valuable to have a sample of data from the final device to determine what kind of bandwidths / sampling rates are necessary.

ADC Distributions



- Nagoya: larger gain for the external amplifier
- Hawai'i: recorded every waveform (even if no signal)

ADC vs TDC Distributions

- Nagoya: time-walk correction performed
 - time is measured by CFD
 - Hawai'i: no time-walk correction performed
 - time is measured by interpolating the leading edge threshold crossing using waveform data
 - 571hreshold set to 50% of the peak voltage for each event

Single Photon Timing Resolutions

- Double Gaussian fits to the distribution of calculated times (using 30% of peak voltage method)
- Time resolution is σ of the narrow Gaussian.
- Example fits @ 10 GSa/s downsampling:

Downsampling to 10.0 GSa/s