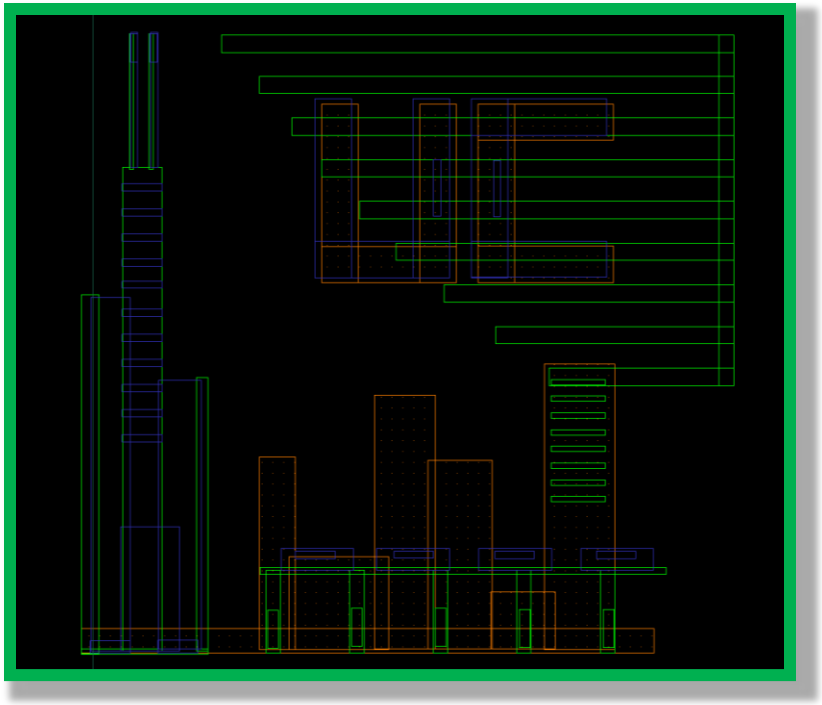
Status/Testing of PSEC-2 Sampling ASIC



JF Genat
Herve Grabas
Eric Oberla

U.S Department of Energy
Argonne NATIONAL LABORATORY
THE UNIVERSITY OF CHICAGO
Office of Science Department of Energy
UNIVERSITY of HAWAI'I MĀNOA

PSEC-2 ”oscilloscope on a chip”

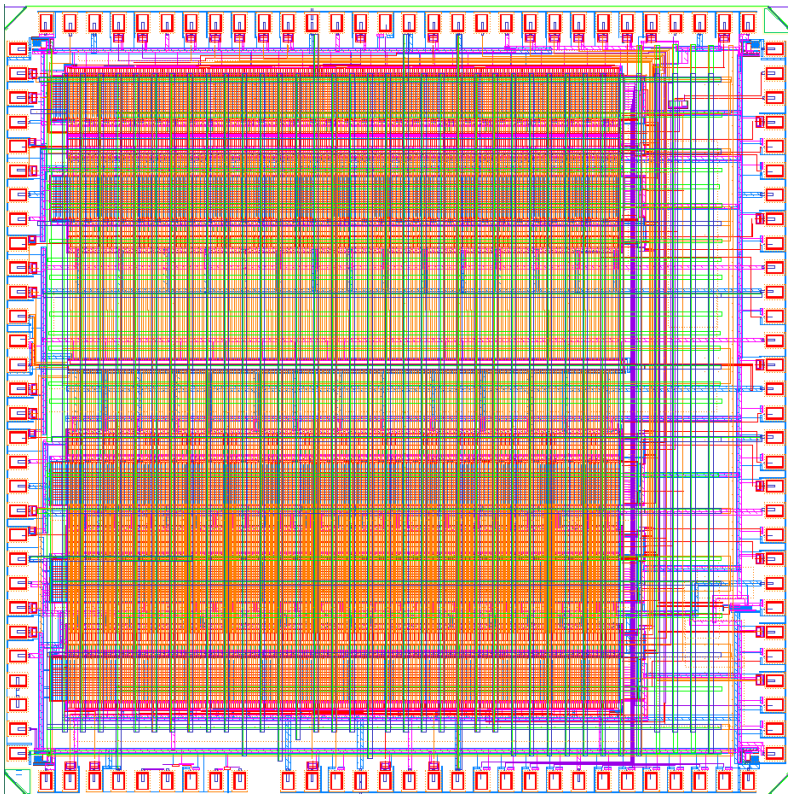
target specs

- channels: **4**
- sampling rate: **5-18 GS/s**
- input bandwidth: **~ 2GHz**
- dynamic range: **1V**
- A/D conversion: **12 bits in 2 µs**
  8 bits in 130 ns
- readout: **6 µs/channel**
- power: **<100mW/channel**
- **Internal trigger**

process

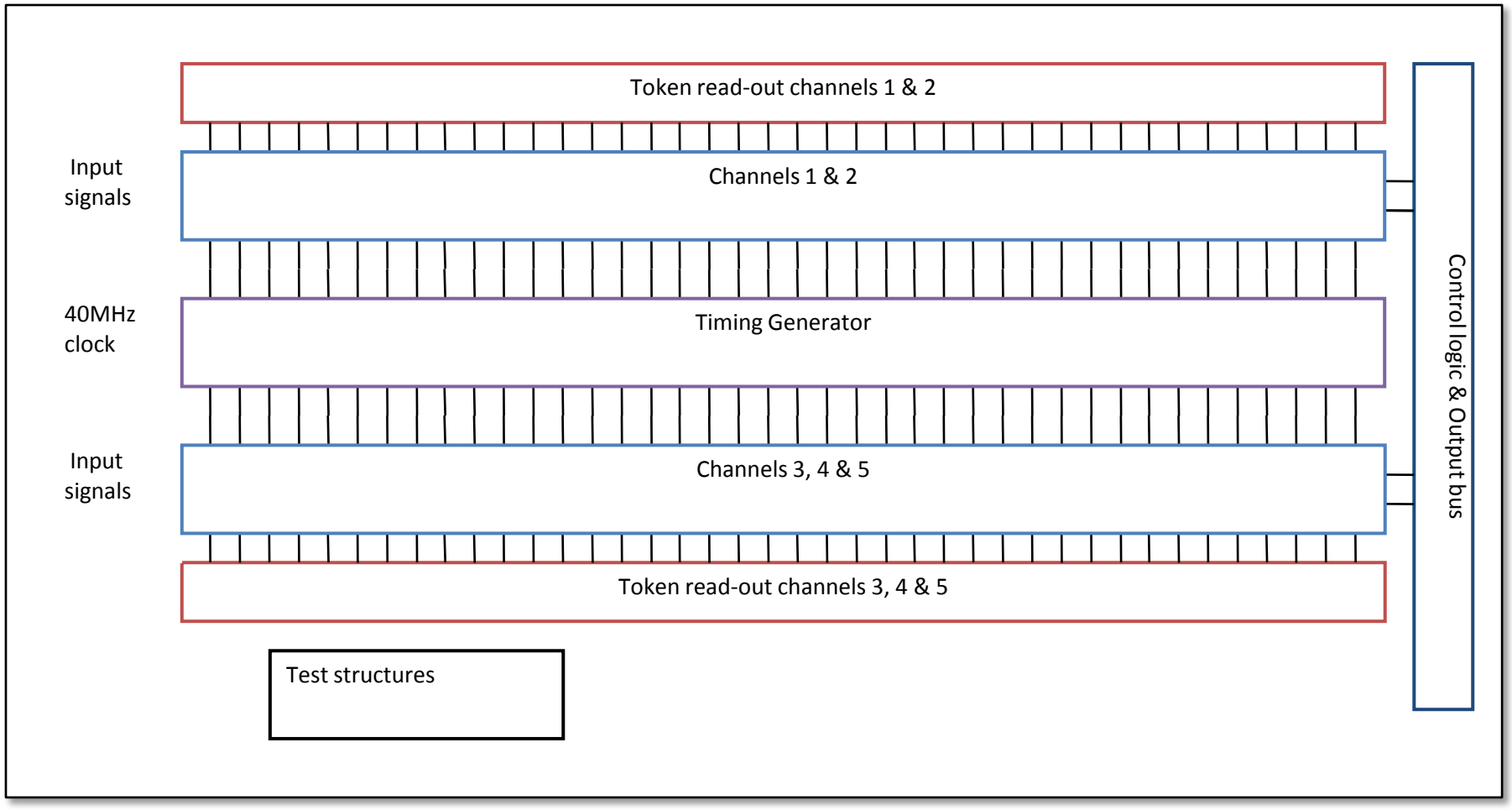
- IBM 130 nm CMOS
- submitted directly to MOSIS
- chip back: Today!

layout



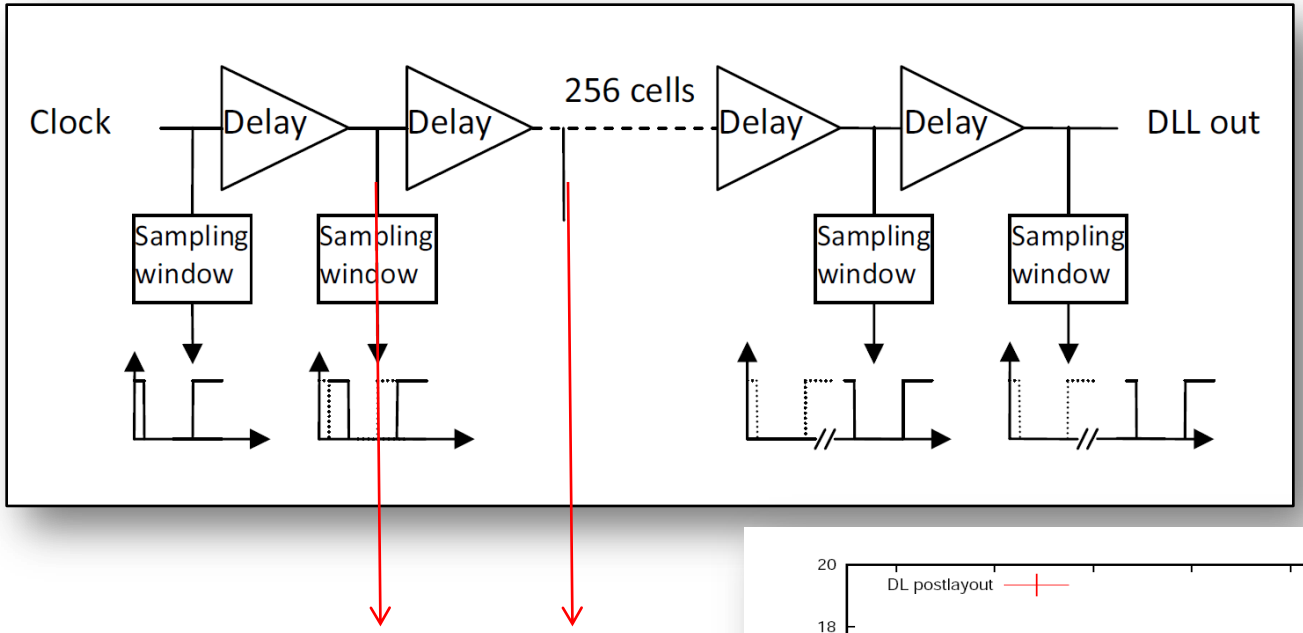
area: 4.4x4.4 mm^2

Principle of Operation



block diagram

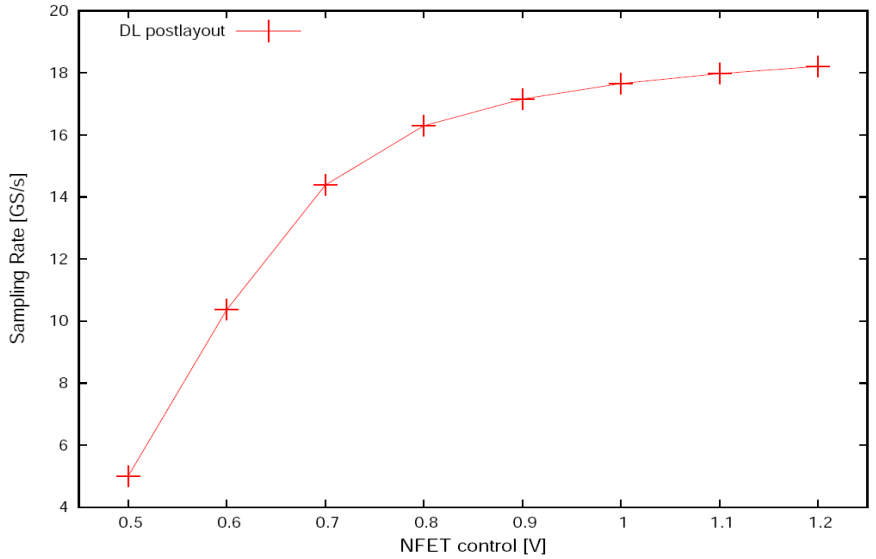
Principle of Operation - timing generator



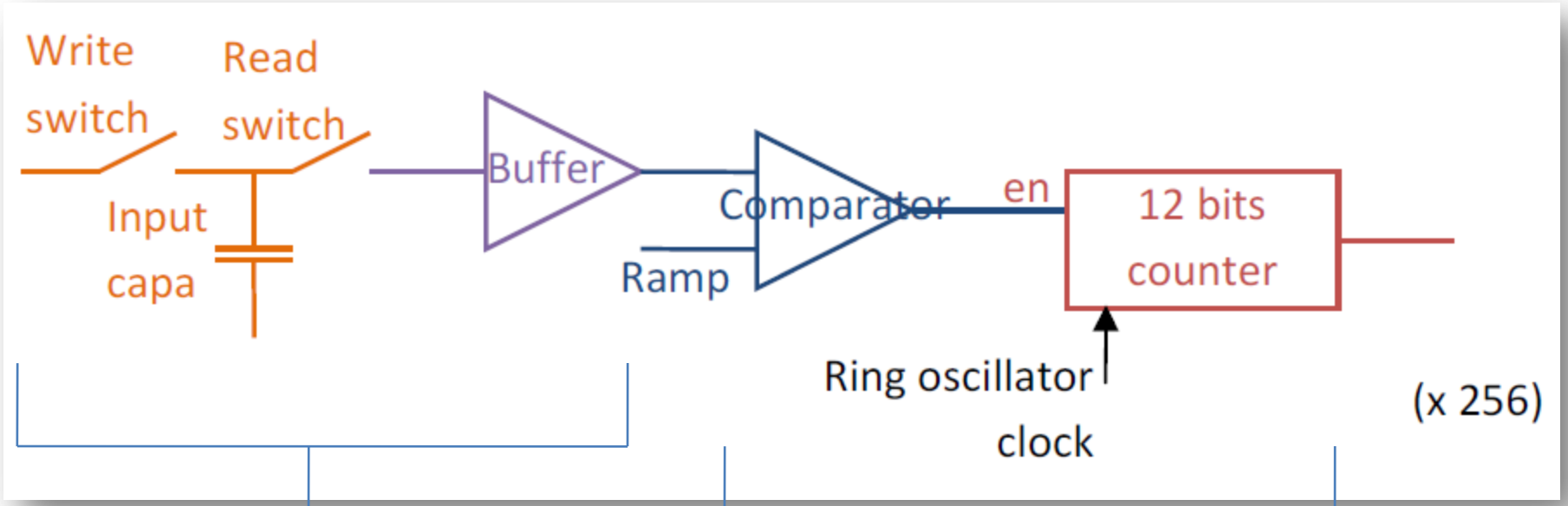
voltage-controlled delay line

delay per cell: Δt

Sampling rate = 1/ Δt



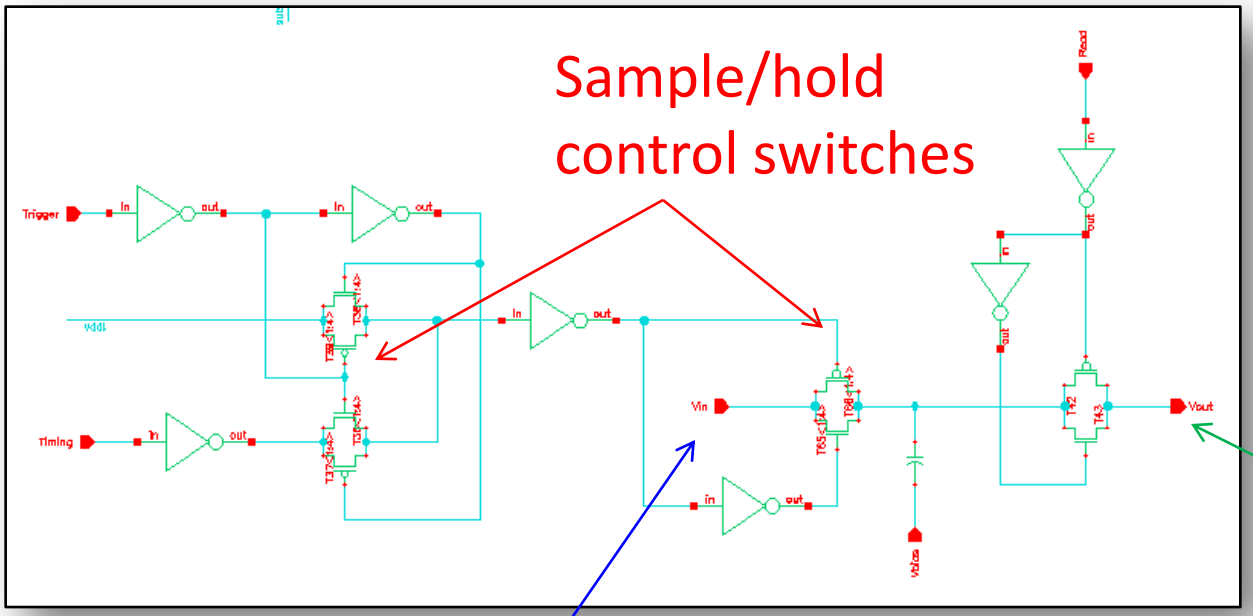
Principle of Operation – channel block diagram



switched capacitor array

Wilkinson ADC

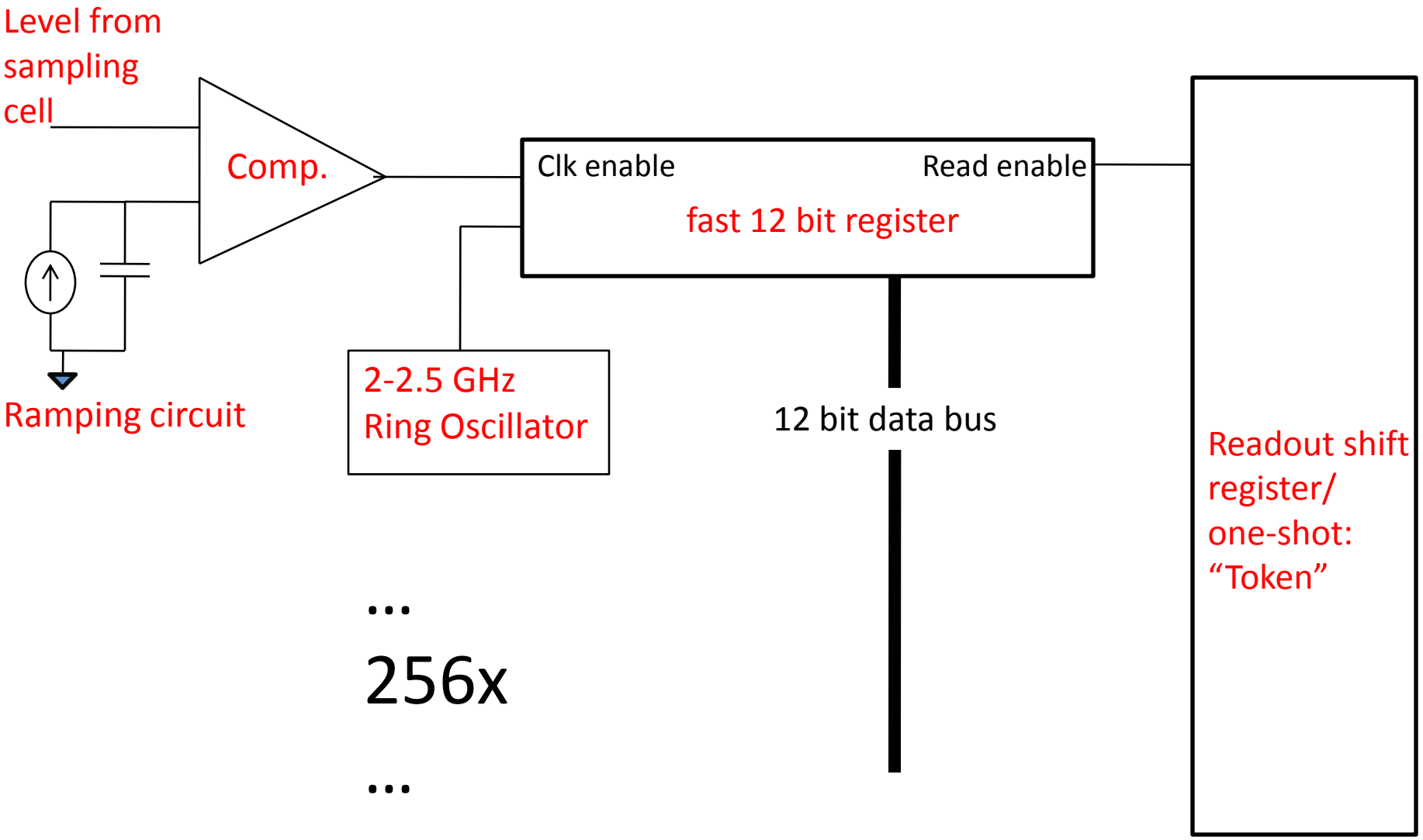
Principle of Operation – switched cap circuit



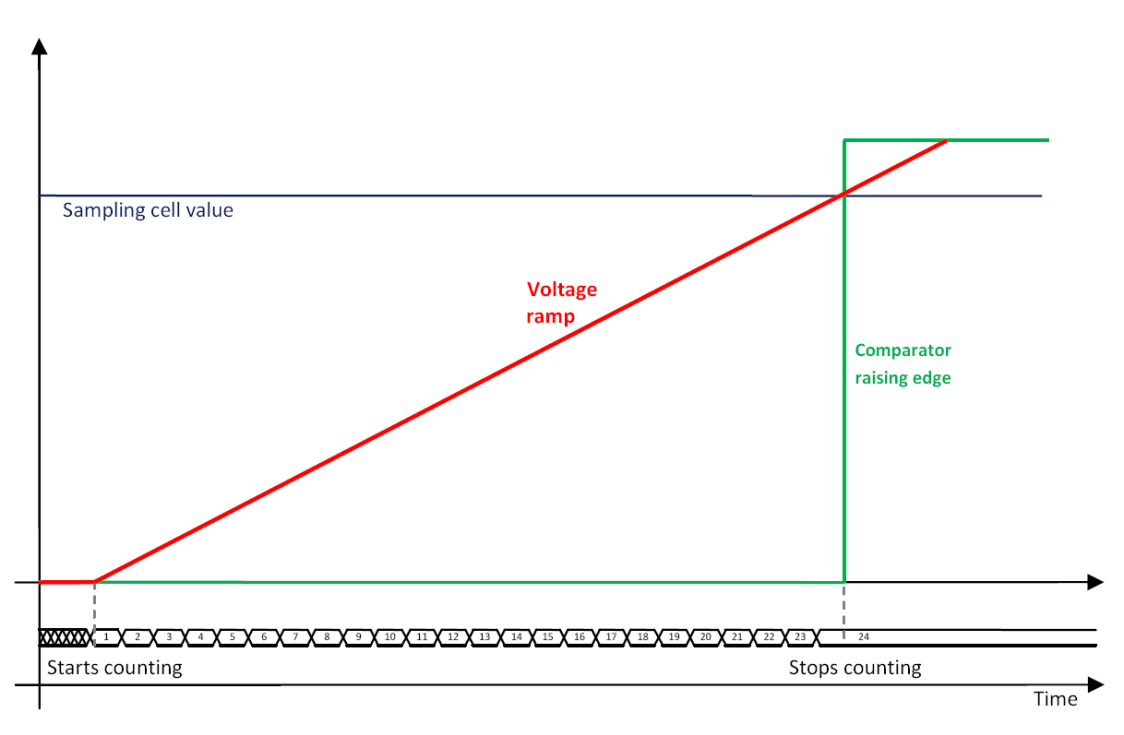
Output to analog buffer→ A/D

Sampled voltage level

Principle of Operation – ADC & Readout

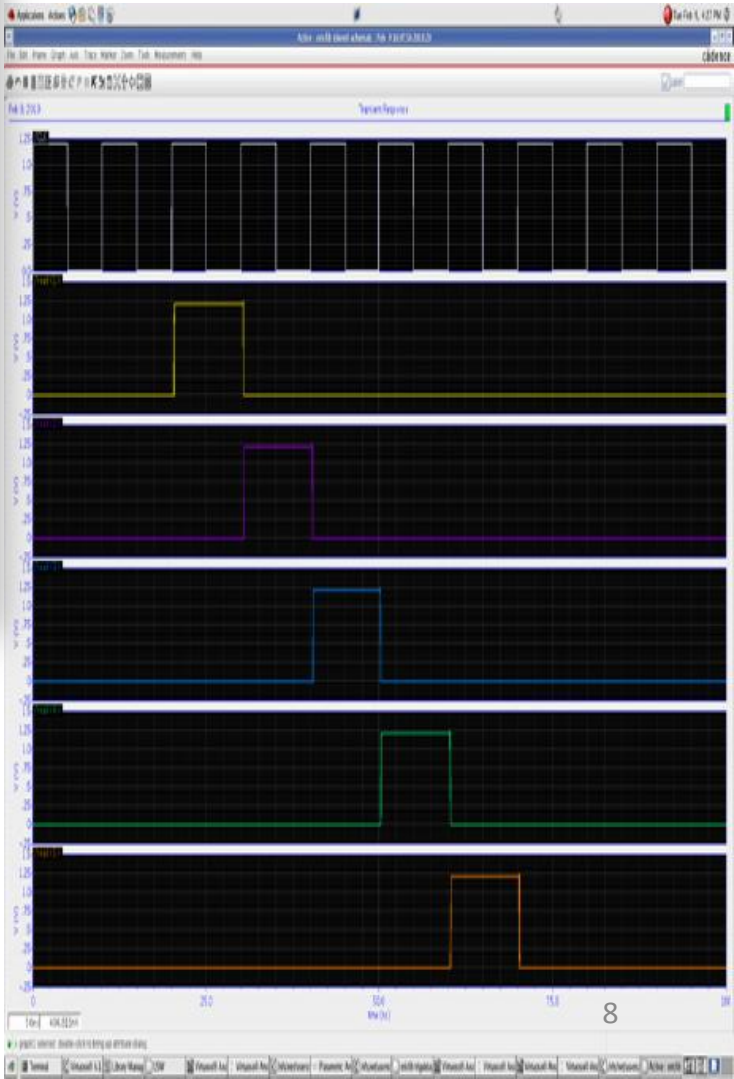


Principle of Operation – ADC & Readout



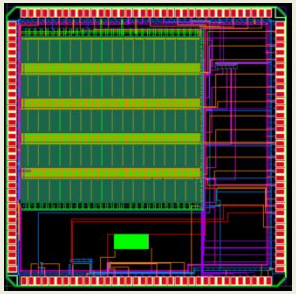
A/D conversion ↑

Token readout →



Evolution

PSEC-1

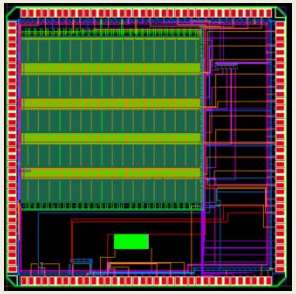


submitted: 7/09

PSEC-1 was overall failure, but we learned a lot
(back-up slides for details)

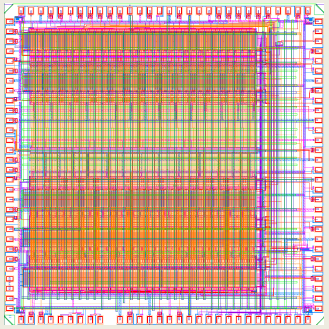
Evolution

PSEC-1



submitted: 7/09

PSEC-2

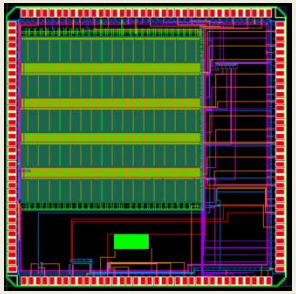


submitted: 2/10

PSEC-1 was overall failure, but we learned a lot
(back-up slides for details)

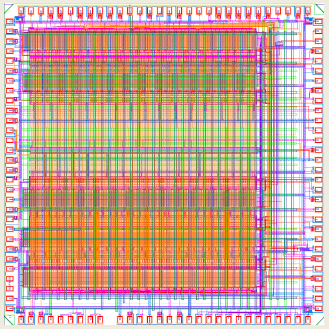
Evolution

PSEC-1



submitted: 7/09

PSEC-2

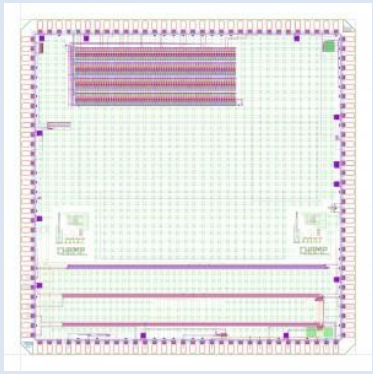


submitted: 2/10

Target next design for specific application
- i.e. event rate/trigger latency/timing needs, etc.

PSEC-1 was overall failure, but we learned a lot
(back-up slides for details)

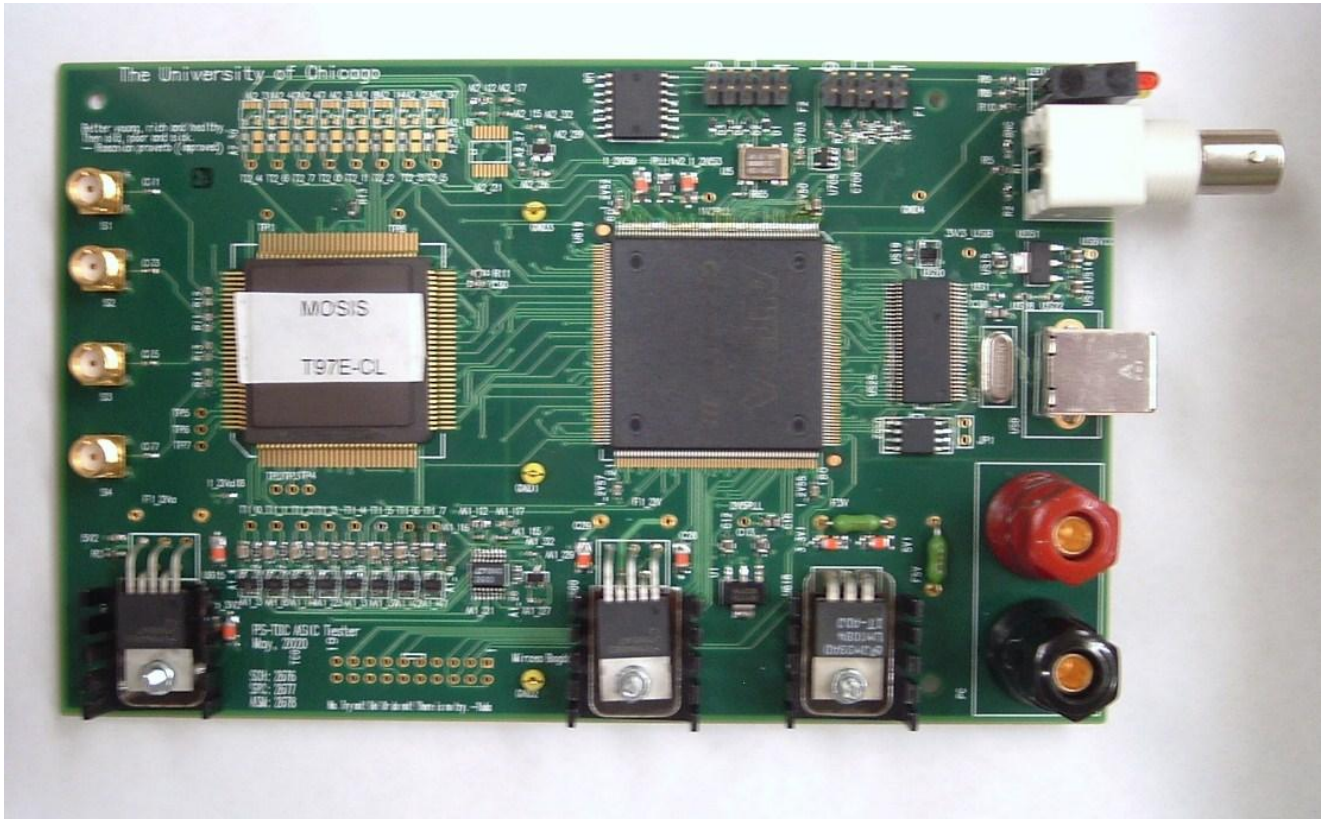
CHAMP



submitted: 5/10

(stay tuned for more info)

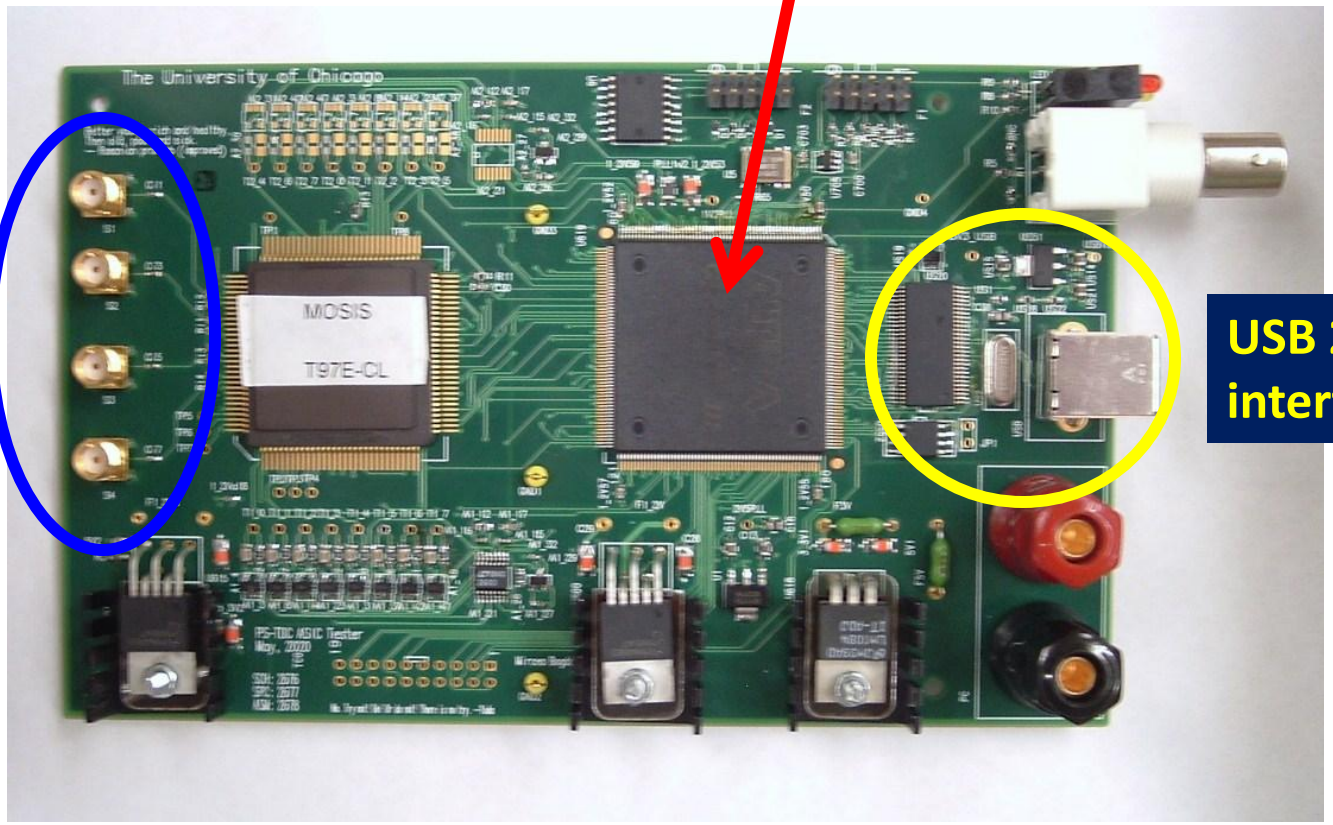
PSEC-2 Evaluation Board



PSEC-2 Evaluation Board

Altera cyclone III

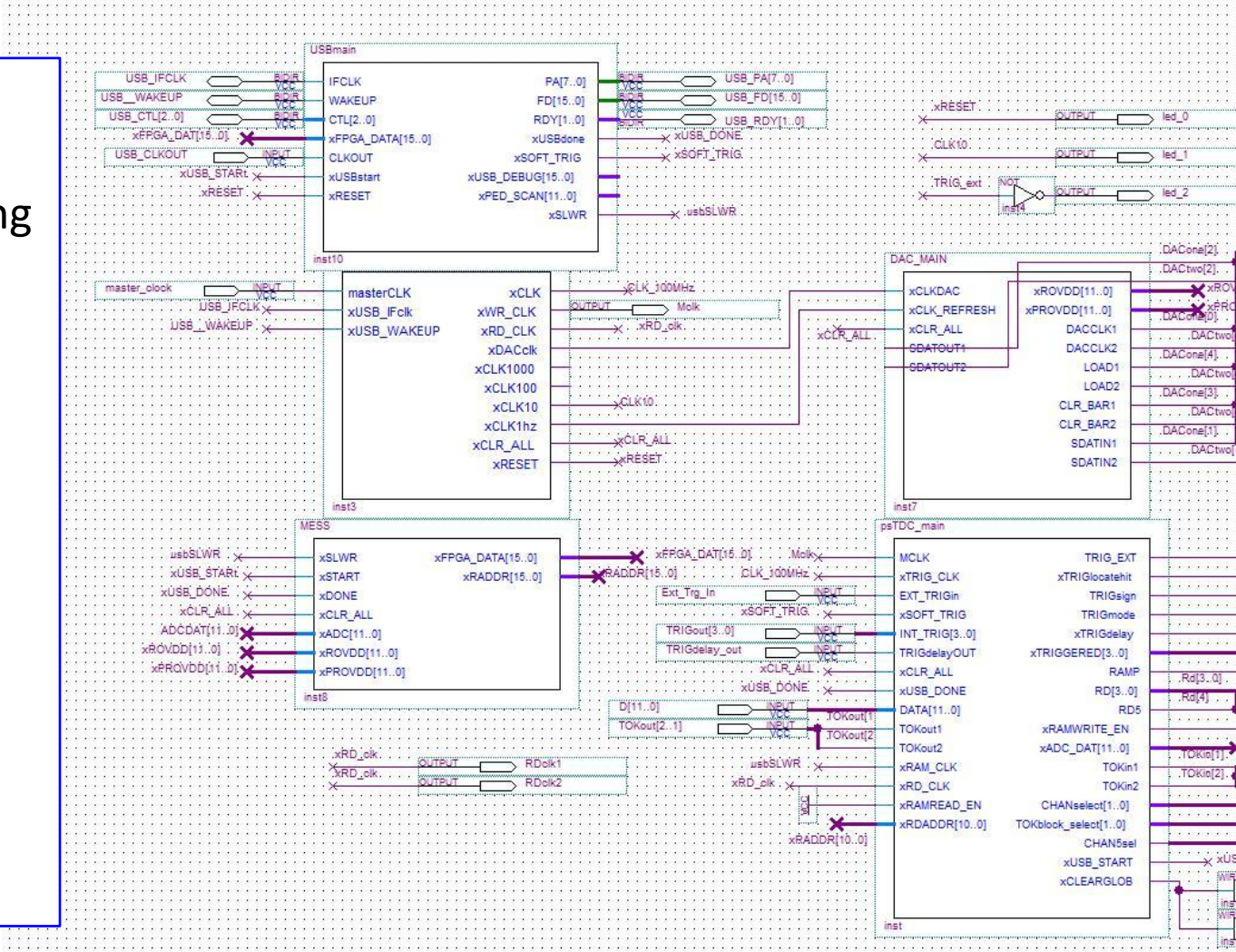
4x SMA inputs



USB 2.0 PC interface

Firmware/Software Status

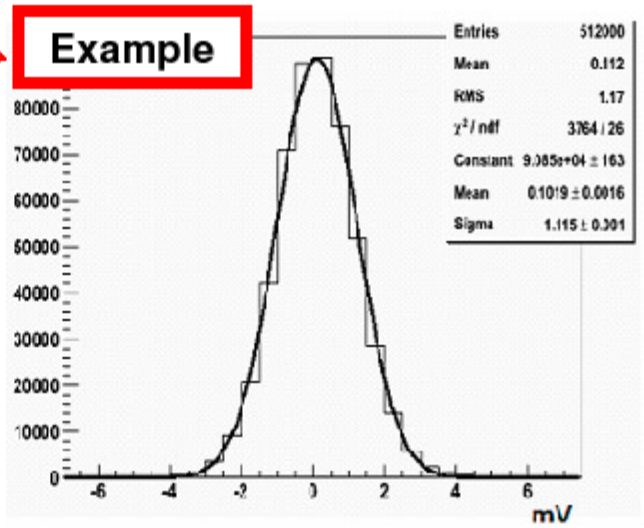
- First revision DONE
- ASIC timing/triggering control
- readout buffer (12x8192 RAM)
- USB firmware driver
- USB software from Hawaii
  - Implement waveform GUI in future



Testing Plans:

Measurement Plans for ASIC Characterization

- <Sample Noise>
- <Leakage Current>
- Analog Bandwidth
- Sampling Speed
- Power Consumption
- Analog/Digital Crosstalk
- **Waveform Timing**
- Test Structures
- DC operating points



from L.Ruckman

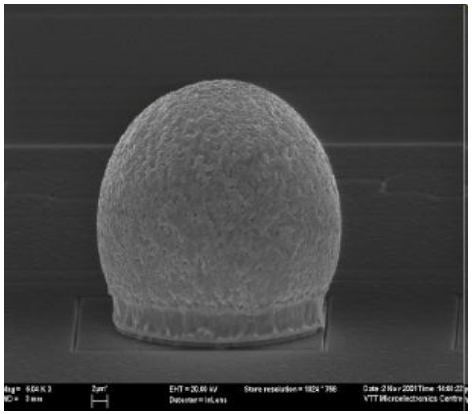
Future Plans

- Parallel development of front-end electronics for MCP 3x2 module

  analog/digital card combo

  stud bonding of bare dies – Aspen Tech.

  detector-electronics integration



- Development of back-end electronics

  coming up in next talks…

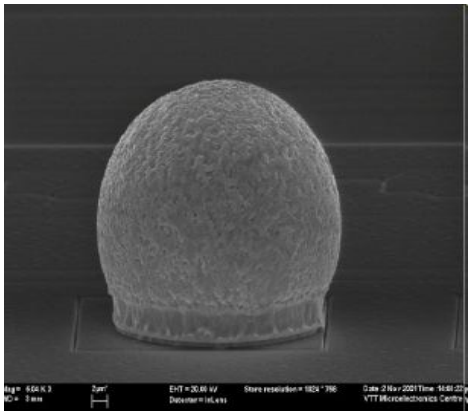
Future Plans

- Parallel development of front-end electronics for MCP 3x2 module

  analog/digital card combo

  stud bonding of bare dies – Aspen Tech.

  detector-electronics integration



- Development of back-end electronics

  coming up in next talks…

- PSEC-3 design down the line..

  PSEC-2 and CHAMP chips need to be tested/understood first

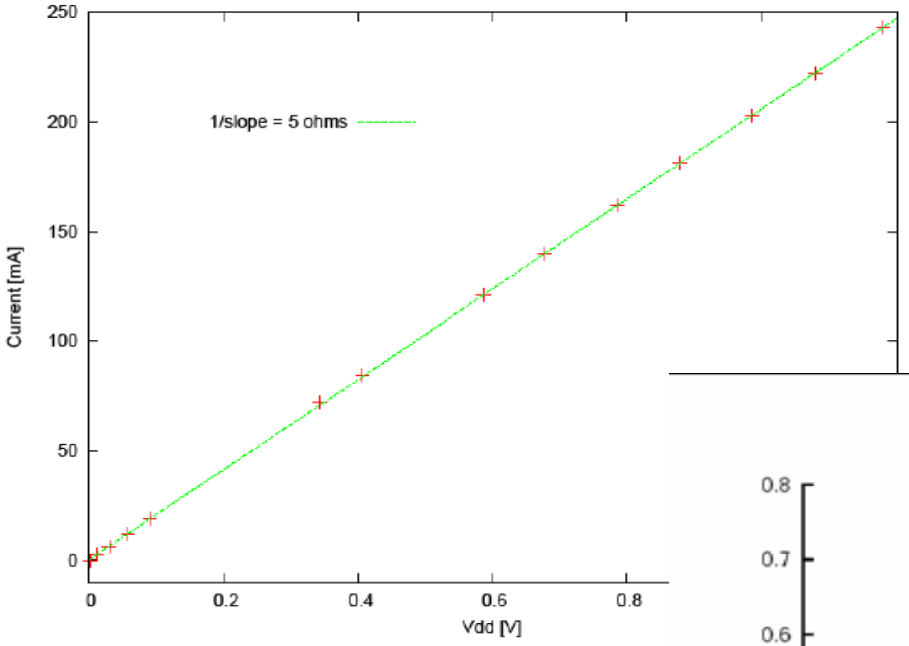
  Design with application in mind?

Summary

- PSEC-2 Eval Board + Firmware is ready
  - need to program FPGA on board
  - 2nd rev. of firmware to be developed as necessary
- USB Software should be ready for testing

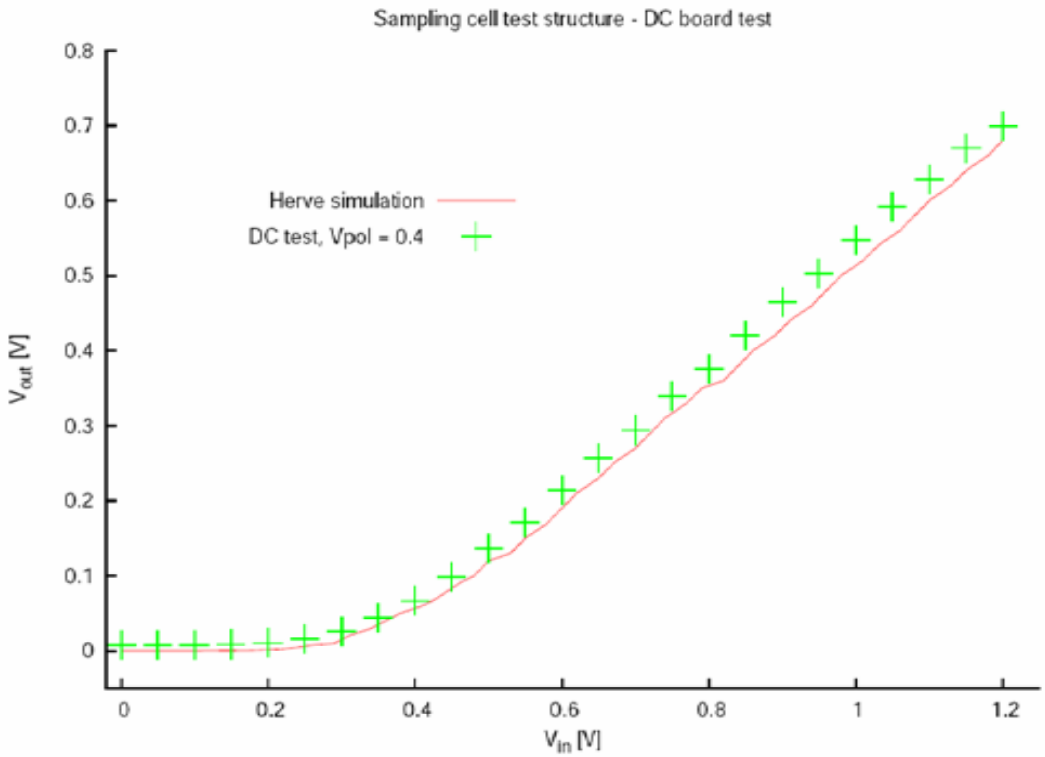
will start PSEC-2 tests next week

Back-up slides (PSEC-1 results)

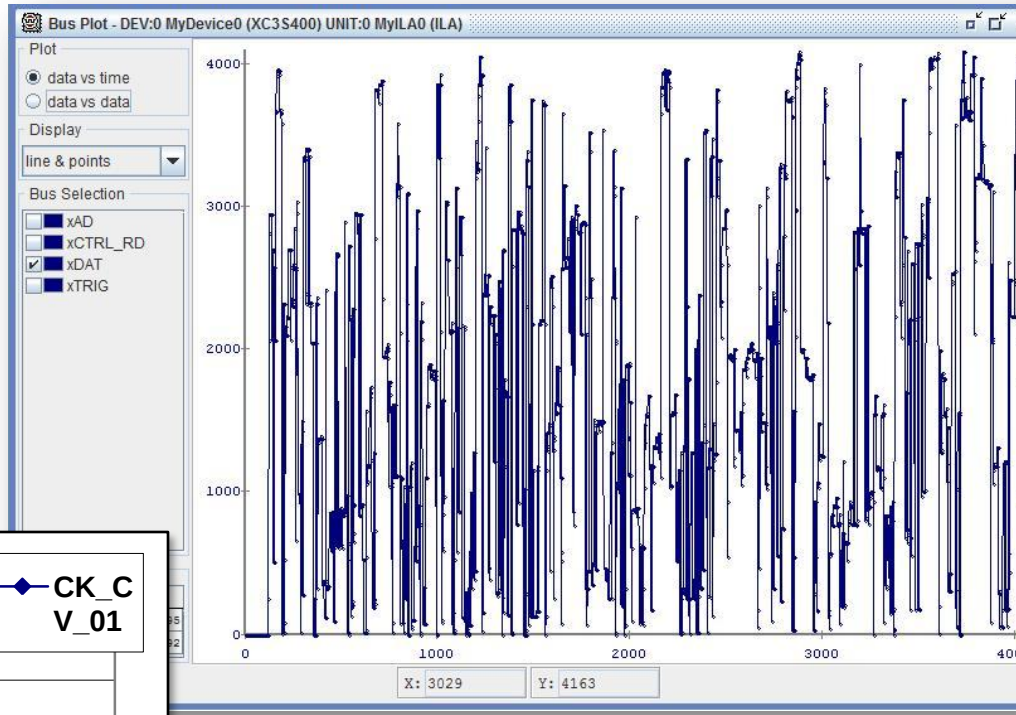


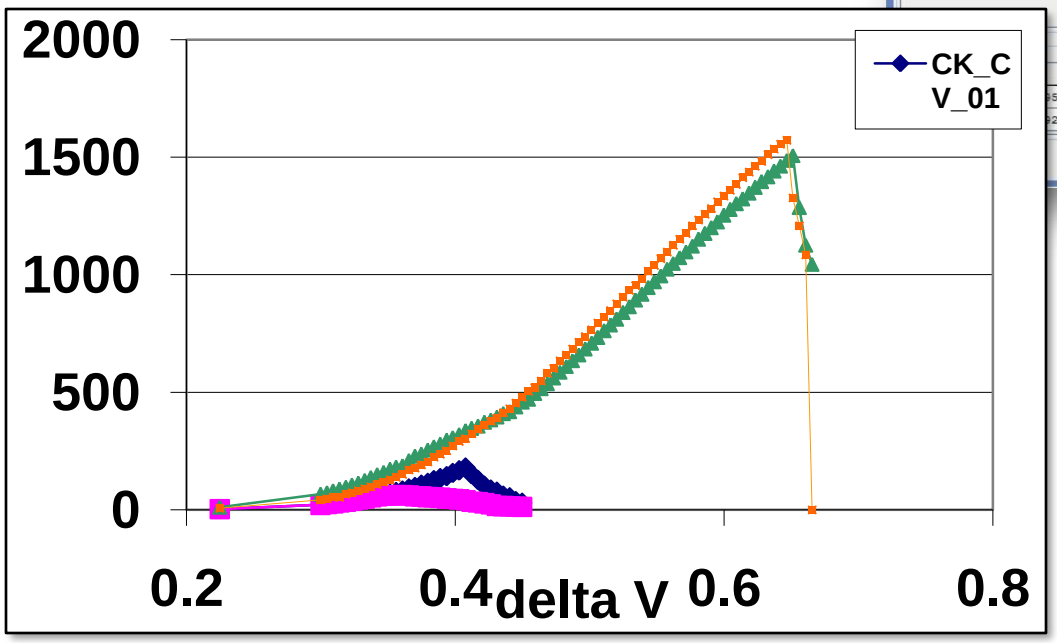
dc current

Sampling cell



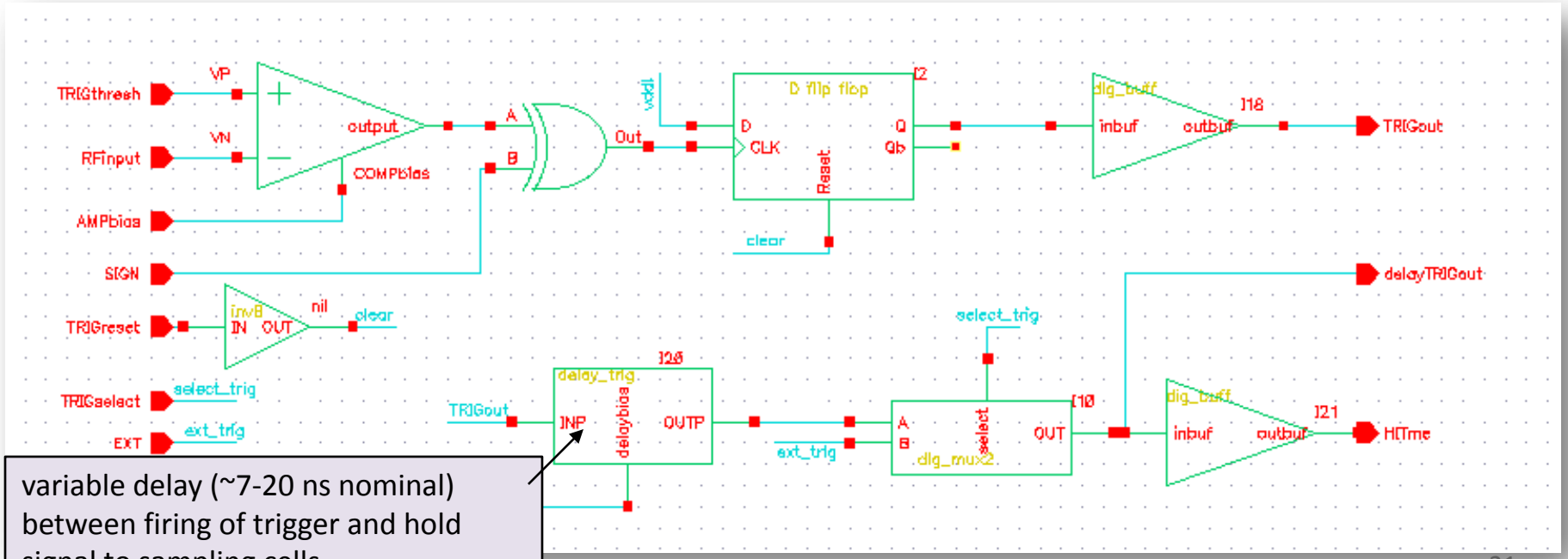
Back-up slides (PSEC-1 results)





Input Trigger

- Positive and negative pulse detection
- Delay before triggering
- Threshold level adjustable
- Bypass possibility



variable delay (~7-20 ns nominal) between firing of trigger and hold signal to sampling cells