PSEC DAQ Central Card– Schedule

Update - 1/24/12

1. Finish Specifications – 11/16/2011;
2. Basic Firmware Design / FPGA Pins – 11/22/2011;
4. Finish Layout/Routing/Artwork – 1/21/2012;
5. Review - 1/19/2012;
6. Recommendations implemented, Artwork regenerated, and PO placed with EPEC 1/23/2012 for 10 pieces PCB;

7. PCB Manufacturing: - 2/17/2012;
8. PCB Assembly (module ready for test) - 3/1/2012.