Status of 1\textsuperscript{st} Generation psTDC ASIC Testing in Hawai’i

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psTDC1 — another “oscilloscope on a chip”

**Specifications**

- 10-15 GSa/s
- >= 2GHz analog bandwidth
- 256 sample cells
- 4 channels
- separate timing channel
- on-chip conversion
- IBM 130nm CMOS process
- 25.6μs readout
- 40mW/channel
- Direct interface (stud-bond) to microstrip board

**Chip Layout**

ASIC due back Oct. 19

Refer to previous presentation
ASIC Evaluation Card (Analog) [A.K.A. “AC card”]

• 1.9 mil (48.26 micron) trace/spacing
  – laser etching
• Fairly $$$ PCB fabrication
• 4x SMA input
• 2x high density Samtec connectors
• Pluggable Mezzanine card
• NP-175 dielectric
Flip Chip Decal (Zoomed In)

\[ Z_0 = 50 \, \Omega \]

\[ R_{\text{term}} = 50 \, \Omega \]
Flip Chip (Stud bonding)

- CVInc has agreed to do the stud bonding on to our PCB
- Lots of European vendors
- Very few USA vendors
ASIC Evaluation Card (Digital)

- 6 mil trace/spacing
- Very cheap PCB fabrication
  - low risk
- 2x high density Samtec connectors
- Analog card’s base board
- USB 2.0 interface
Analog/Digital PCB Combo
Measurement Plans for ASIC Characterization

- Sample Noise
- Leakage Current
- Analog Bandwidth
- Sampling Speed
- Power Consumption
- Analog/Digital Crosstalk
- Waveform Timing
Firmware Status: Basically Done

- State machine for ASIC Wilk. ADC conversion
- USB firmware driver
- Real-time digital logic verification w/ Chipscope
- Temperature compensation control loops
What’s next after ASIC Evaluation Phase?

• Instrument ASIC to a MCP photodetector
• Development of backend electronics
• Develop a $2^{nd}$ generation psTDC ASIC
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Concept Drawing

Chicago Version

Hawaii Version

Refer to the presentation by Herve Grabas
ps Laser Setup in Hawai‘i

- 2-D scanning area
- \( \sim 2 \text{ps RMS Pilas} \)
- 405nm pulsed laser
- Cross-talk scanning capabilities
  - Adjacent MCP pads channels
What’s next after ASIC Evaluation Phase?

- Instrument ASIC to a MCP photodetector
- **Development of backend electronics**
- Develop a 2\textsuperscript{nd} generation psTDC ASIC
Employ compact PCI experience

cPCI crate

cPCI CPU

XMC card
XMC/PMC card

Effective 1 GB/s throughput

4x 3Gbps Fiber inputs

Direct transfer to RAM with DMA

For raw waveform logging only (no online data processing)
- 500 MHz processor per core
- Real-time feature extraction
- Reduce data volume rate

DSP_FIN

4x Fiber Optic Connections

3.00 GB/s

Dual Core DSP

128 MB SDRAM
What’s next after ASIC Evaluation Phase?

• Instrument ASIC to a MCP photodetector
• Development of backend electronics
• **Develop a 2\textsuperscript{nd} generation psTDC ASIC**
2\textsuperscript{nd} Generation psTDC ASIC

- Too premature to make too many comments
- Possible improvements and/or additional features:
  - Internal PLL
  - On-chip discriminators
  - Deeper analog buffering
  - Increase number of input channels
Summary/Status for the Hawai’i Effort

• Analog Evaluation PCB
  – part kit and 5x PCBs @ assembly house
  – Waiting for bare dies from MOSIS

• Digital Base Board
  – Ready!

• FPGA Firmware
  – Ready!

• USB Software
  – Basically done, except need to add waveform GUI
Backup Slides
LAPPD Front-end Electronics studies

1GHz analog bandwidth, 5GSa/s

Simulation includes MCP response

G. Varner and L. Ruckman

J-F Genat, G. Varner, F. Tang, H. Frisch
Concept Drawing

- “pluggable” board design
- Multiple testing configurations
Test #1

• Verify glass micro-strip waveguide with compression bracket and MCP
• Get frequency response for MCP, glass TX-line, bracket, and Roger component
• Get channel cross-talk (radiative) frequency response
Test #3

- Use a ultra-low jitter laser light (signal photon level) to measure ASIC waveform timing
Basic Electrical Outline for FPGA Interface

- Stud Bonding
- Common CLK
- Multiple PC interfaces