Electronics Testing at UC

Eric Oberla
University of Chicago

LAPPD Collaboration Meeting, October 16-17 2009,
Argonne National Laboratory
Sampling ASIC

- 40 MHz write clock to timing generator
  - Output sampling window to storage cells
  - Controls write switch to sampling capacitors

- A/D conversion with 500 MHz-2GHz RO
  - 12 bit, 256 conversions in parallel

- 40 MHz read clock to Readout Token
  - Serial readout of data to output bus
Test Boards

- Bare Die (30 chips)
- Ceramic package (10 chips)

AC Test Board
Designed by Hawaii

DC Test Board
Designed by Chicago

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Test Boards

4x SMA inputs

AC Board

bare die

FPGA

Logic signals and outputs using LEMO I/Os

Analog voltage control by potentiometer

Packaged Chip

DC Board
DC Board

Why a DC board?

- Bonding of bare die to AC card is $$$$, need to make sure it’s a good investment. DC board is simple and relatively cheap.

- Measure power, DC operating points

- Also, we included several ‘test structures’ on chip
  - Comparator
  - Sampling Cell
  - Ring Oscillator w/ 12 bit counter

Compare results to simulation
DC Board Tests

- **DC Tests**
  - ‘Smoke test’ – turn on power
  - Measure power dissipation, DC operating points

- **Low-level AC tests**
  Comparator (ADC) – response time, operating range
  Ring Oscillator – frequency range
  Sampling cell – DC characteristics
  Ramp – linearity
  Token – does it work?

*simulation*
Test Setup
Plans

- Chip due back Monday (10/19) + DC board due back today = Results next week (?)

  - Complete DC tests
  - Tests using AC card in coordination with Hawaii

  Full chip characterization:

  - Analog Bandwidth
  - Sampling rate
  - etc…

  Firmware written by Larry Ruckman