Status/Testing of PSEC-2 Sampling ASIC

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PSEC-2  "oscilloscope on a chip"

**target specs**

- channels: 4
- sampling rate: 5-18 GS/s
- input bandwidth: ~ 2GHz
- dynamic range: 1V
- A/D conversion: 12 bits in 2 µs
  8 bits in 130 ns
- readout: 6 µs/channel
- power: <100mW/channel
- Internal trigger

**process**

- IBM 130 nm CMOS
- submitted directly to MOSIS
- chip back: Today!

area: 4.4x4.4 mm²
Principle of Operation

Token read-out channels 1 & 2

Channels 1 & 2

Timing Generator

Channels 3, 4 & 5

Token read-out channels 3, 4 & 5

Input signals

40MHz clock

Test structures

Control logic & Output bus

block diagram
Principle of Operation - timing generator

Delay per cell: $\Delta t$

Sampling rate = $1/\Delta t$

Voltage-controlled delay line
Principle of Operation – channel block diagram

- Write switch
- Read switch
- Input capa
- Buffer
- Comparator
- Ramp
- 12 bits counter
- Ring oscillator clock (x 256)

Switched capacitor array

Wilkinson ADC

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Principle of Operation – switched cap circuit

Sample/hold control switches

Sampled voltage level

Output to analog buffer → A/D
Principle of Operation – ADC & Readout

Level from sampling cell

Comp.

Ramping circuit

2-2.5 GHz Ring Oscillator

Clk enable

fast 12 bit register

Read enable

Readout shift register/one-shot: “Token”

12 bit data bus

... 256x ...

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Principle of Operation – ADC & Readout

A/D conversion

Token readout

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PSEC-1 was overall failure, but we learned a lot
(back-up slides for details)
Evolution

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PSEC-1 submitted: 7/09

PSEC-2 submitted: 2/10

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Evolution

PSEC-1 was overall failure, but we learned a lot (back-up slides for details).

Target next design for specific application
- i.e. event rate/trigger latency/timing needs, etc.

PSEC-1 submitted: 7/09
PSEC-2 submitted: 2/10

CHAMP submitted: 5/10

(stay tuned for more info)

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PSEC-2 Evaluation Board
PSEC-2 Evaluation Board

- Altera cyclone III
- USB 2.0 PC interface
- 4x SMA inputs
Firmware/Software Status

- First revision DONE
- ASIC timing/triggering control
- readout buffer (12x8192 RAM)
- USB firmware driver
- USB software from Hawaii
  Implement waveform GUI in future

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Testing Plans:

Measurement Plans for ASIC Characterization

- Sample Noise
- Leakage Current
- Analog Bandwidth
- Sampling Speed
- Power Consumption
- Analog/Digital Crosstalk
- **Waveform Timing**
  - Test Structures
  - DC operating points

from L.Ruckman
Future Plans

• Parallel development of front-end electronics for MCP 3x2 module analog/digital card combo
  stud bonding of bare dies – Aspen Tech.
detector-electronics integration

• Development of back-end electronics
  coming up in next talks...
Future Plans

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• PSEC-3 design down the line..
  PSEC-2 and CHAMP chips need to be tested/understood first
  Design with application in mind?
Summary

• PSEC-2 Eval Board + Firmware is ready
  - need to program FPGA on board
  - 2nd rev. of firmware to be developed as necessary

• USB Software should be ready for testing

will start PSEC-2 tests next week
Back-up slides (PSEC-1 results)

- dc current

- Sampling cell
Back-up slides (PSEC-1 results)
Input Trigger

- Positive and negative pulse detection
- Delay before triggering
- Threshold level adjustable
- Bypass possibility

Variable delay (~7-20 ns nominal) between firing of trigger and hold signal to sampling cells