PSEC-4 Waveform Digitizing ASIC + Analog Card
Front-end of SuperModule DAQ system

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LAPPD collab meeting III
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PSEC-4

- Waveform digitizing ASIC
- Sampling rate capability > 10GSa/s
- Analog bandwidth > 1 GHz
- Medium event-rate capability (up to ~100 KHz)

**ACTUAL PERFORMANCE**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling Rate</td>
<td>2.5-15 GSa/s</td>
</tr>
<tr>
<td># Channels</td>
<td>6</td>
</tr>
<tr>
<td>Sampling Depth</td>
<td>256 points (17-100 ns)</td>
</tr>
<tr>
<td>Input Noise</td>
<td>&lt;1 mV RMS</td>
</tr>
<tr>
<td>Analog Bandwidth</td>
<td>1.6 GHz</td>
</tr>
<tr>
<td>ADC conversion</td>
<td>Up to 12 bit @ 1.5 GHz</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>0.1-1.1 V</td>
</tr>
<tr>
<td>Latency</td>
<td>2 µs (min) – 16 µs (max)</td>
</tr>
<tr>
<td>Internal Trigger</td>
<td>yes</td>
</tr>
</tbody>
</table>
PSEC-4
PSEC-4 architecture

Timing generation with a delay locked loop (DLL):

- 1536x parallel Wilkinson ADC (entire chip)
- Region of interest readout (40 MHz) -> data to FPGA
Evaluation Card

- 4 boards made (3 available in this time zone)
  - 6 channels (1 PSEC-4) per board
- **USB 2.0 interface**
  - Current firmware revision – 2
  - Acquisition software available with oscilloscope GUI
PSEC-4 Performance

**Noise**

- Low noise <1 mV
- ~1V dynamic range with excellent linearity
- Analog bandwidth of 1.6 GHz
- Sampling rates up to 15 GSa/s

**Frequency Response**

$\sigma \sim 0.75\text{mV}$

$f_{3\text{dB}} = 1.6\text{ GHz}$

**DC Response**
PSEC-4 timing (preliminary)

- Without time base calibration (assuming nominal 100 ps per sample interval)
- Time jitter measured at DLL output ~ 13 ps
- Sample several hundred Gaussian waveforms on 2 channels:

![Data from 1 channel shown]
PSEC-4 timing (preliminary)

- Without time base calibration (assuming nominal 100 ps per sample interval)
- Sample several hundred Gaussian waveforms on 2 channels:

**2 channel timing (window subset - 3.8ps sigma)**

Working out various time-base calibration methods with Kurtis Nishimura (UH) -- should be implemented soon!
Argonne Test Stand

• Working to implement PSEC-4 eval at laser lab (APS)

First pulses from 33mm MCP set-up captured with PSEC-4 @ 10GS/s
Argonne Test Stand

- Some 33 mm MCP pulses:

- Still some noise/triggering issues to resolve before using PSEC-4 data for analysis. Coming soon...
Analog Card

- 30 chan. PSEC-4 readout board, input matched to 30 strip anode
- Digital I/O and Power thru 240 pin SAMTEC (→ digital card)

--boards due back next week--
Analog Card

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--boards due back next week--
Analog Card → Super Module

Analog Card – 5 PSEC-4 ASICs (30 channels)
- system ABW ~ 1 GHz (anode limited)
- 4 Analog Cards per module
- flexibility allows for integration of alternative front-end ASICs
Analog Card ➔ Super Module

Analog (blue)+ Digital (yellow) cards mechanical mounting

Drawing courtesy of Rich Northrup
Summary/plans

• PSEC-4 performance meets initial project goals of a (functional) high bandwidth, fast sampling ASIC
• Continued performance testing → paper
• More data runs w/ 33mm & 8 inch MCP setup
  - Integration of PSEC-4 data into analysis pipeline
  - Any necessary firmware improvements
  - Start PSEC-4/scope analysis comparison
• **Analog Card** back next week – waiting on digital card for full system testing, but preliminary tests/integration by the end of the year
• PSEC-5? Adding a deeper buffer and faster readout speed desired (reduce chip deadtime)
DAQ system

• Backside of Super Module:

**Digital Card** – 4 per module
- PSEC-4 control, trigger handling, & calibration
DAQ system

- Backside of Super Module:

- Data + System Clock + Ctrl

- Gigabit Ethernet

Center Card
- System control
- Clock distribution
- Feature extraction
- CPU interface
Switched Capacitor Array Sampling

Write pointer passed along array - generates ‘sampling window’ (~5-10 switches closed at once):

Timing generation with a delay locked loop (DLL):

Locked sampling @ 10GSa/s w/ on-chip DLL

To switched capacitor array – sample & hold
Wilkinson ADC – easy to integrate on-chip