Supermodule Software, Firmware & DAQ

Edward May
3rd LAPPD Collaboration Meeting
Argonne National Lab, 9-10 Dec 2011
Supermodule: Hardware View

Beam Test Configuration

Existing modules:
- Analog Card Rev A: PSEC3
- Digital Card Rev A: 1 piece PSEC3

New modules:
- Analog Card Rev B:
  - Change to PSEC4
- Digital Card Rev B:
  - Change to 5 pieces PSEC4
- Center Card: new design.
Super Module and other targets for DAQ software

- 8” detector module (60 channels)
- 2x3 Super Module panel (120 channels)
- Test beam modules (>= 120 channels)
- Daniel Boone Detector prototype (2400 channels)
Documentation (needs work)

- Requirements
- Architecture
- Hardware Design
- Software API's
Data Flow

DC FPGA

CC FPGA

DAQ PC

Disk

Nearline/Offline

Configuration Calibration

raw data

low-level features

raw data

high-level features

raw data

raw data

feature data

special data

Configuration Calibration Control

Presenter, Histogrammer, Archive Builder
Functionality, Versioning and Coordination

- Digital Card FPGA
  - V0: 4 channel support (Evaluation board)
  - V1: 30 Channel support
    - IN: pedestals, channel mapping, configuration information
    - rOUT: address labeling, raw data, status information, error notification, checksums, standalone communication with DAQ PC
  - V2
    - IN: adds charge and time calibration
    - OUT: adds sparse data, local feature extraction

- Center Card FPGA

- DAQ Personal Computer
  - V0: Pedestals, Raw data to disk
  - V1: Configuration, calibration, run database; channel to real space mapping, raw data and feature histogramming, run control, polling synchronization, error control
  - V2 High Voltage Control and monitoring,

- Nearline/Offline
# Projects, Developers and Schedule

## Hardware View

<table>
<thead>
<tr>
<th>Project Name</th>
<th>Developer</th>
<th>Date Version 1 Available</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Card w/PSEC4</td>
<td>Eric Oberla</td>
<td>9 Jan 2011</td>
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<tr>
<td>Digital Card</td>
<td>Craig Harabedian</td>
<td>1 Mar 2011</td>
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<tr>
<td>Center Card</td>
<td>Mircea Bogdan</td>
<td>1 Mar 2011</td>
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## Projects, Developers and Schedule

### Software View

<table>
<thead>
<tr>
<th>Project Name</th>
<th>Developer(s)</th>
<th>Date Version 1 Available</th>
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<tbody>
<tr>
<td>Digital Card Firmware</td>
<td>Aaron Meyer</td>
<td>V.0 exists for 4ch Eval Board</td>
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<tr>
<td></td>
<td>Eric Oberla</td>
<td>V.1 needed by 1 Mar 2011</td>
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<tr>
<td>Center Card Firmware</td>
<td>Maxwell Hutchinson</td>
<td>V.1 needed by 1 Mar 2011</td>
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<tr>
<td></td>
<td>Craig Harabedian</td>
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<tr>
<td>DAQ computer Code</td>
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<td>V.0 exists for 4ch Eval Board</td>
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<td>V.1 needed by 1 Mar 2011</td>
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<td>Calibration Software</td>
<td>Kurtis Nishimura</td>
<td>V.0 exist for time only offline version</td>
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<td>Nearline/Offline code</td>
<td>Matt Wetstein</td>
<td>V.0 exists</td>
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<td></td>
<td>Razib Obaid</td>
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<td></td>
<td>Alexander Vostrikov</td>
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<td>Andre Elagin</td>
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Conclusions & Summary

- Clear needs and schedule
- Sufficient Effort to meet schedule
- Needs organization and documentation