LAPPD Electronics Integration Godparent Review
Committee Report and Recommendations
July 19, 2012

The fourth godparent review of the LAPPD electronics and integration was held at Argonne on July 9, 2012. The reviewers were:

Bernhard Adams, ANL
Marcel Demarteau, ANL
Gary Drake, ANL (chair)
Sten Hanson, FNAL
Antonino Miceli, ANL
Igor Veryovkin, ANL

The presentations given at the review were as follows:

1. Electronics Overview and Review of May 2011 Items - Gary Varner, Univ. of Hawaii

2. Signal Development and Coupling to Readout Electronics - Razib Obaid, Univ. of Chicago

3. PSEC4 ASIC Status - Eric Oberla, Univ. of Chicago

4. Alternative ASIC Options - Kurtis Nishimura, Univ. of Hawaii

5. Glass Tile Readout System Status - Mircea Bogdan, Univ. of Chicago

6. Ceramic MCP Readout System Status - Matt Andrew, Univ. of Hawaii

7. Data Processing & Calibration - Kurtis Nishimura, Univ. of Hawaii

8. System Test at APS and Software/Data Archiving - Matt Wetstein, Univ. of Chicago

9. Schedule & Plans - Henry Frisch, Univ. of Chicago

10. Going forward: discussion items - Gary Varner, Univ. of Hawaii

The committee was generally very impressed with the progress in the electronics development and the overall state of this part of the project. The committee feels that the electronics development is generally in good shape for the upcoming DOE reviews, and that the group should be able to complete the remaining work to meet the project milestones for the electronics by the end of the fiscal year. We have a few specific comments and suggestions for meeting the goals for this phase of the project. We also offer comments and suggestions for planning a second phase of the project, which

presumably will focus on specific applications. While our purview is the electronics, because this is a highly-integrated system, some of our comments touch on other areas. We offer our comments and suggestions below:

1. The overall architecture of the readout system is very well conceived for this stage of the project. It is general enough to be useful in studying a number of applications that might have different performance requirements. The variety of interface features and timing options are what is needed right now to get photo-detector samples into the hands of potential customers and users. We strongly recommend that this aspect be highlighted in a significant way in future presentations and reviews, as we believe it to be one of the key points of this development. One consequence of generality however is having more features than needed for a specific application (e.g. Ethernet, USB, QSFP fiber, different timing options, etc.). Another is increased power consumption. While these are useful for R&D and this phase of the project, we presume that for the next phase, designing for a specific application will narrow the focus and requirements toward an efficient set of features optimized for that application. This should result in a more compact package design, lower power consumption, etc. We recommend that the group give careful thought to this in preparing for the next phase of the project and proposals, as well as upcoming reviews. In particular, we suggest that this set of electronics not be advertised as "one size fits all," since it is clear that improvements in certain areas can be achieved at the expense of others. (For example, a water Cherenkov detector would want ~100 pSec timing resolution and low power consumption, but the amount of material in the packaging is not important. For a TOF detector, 1 pSec timing resolution is needed, the power consumption is less important, but the packaging and mass is critical...)

2. To meet the near-term milestone of the project (i.e. the official end of this phase of the project with the deadline of Sept. 30, 2012), the committee believes that the most important aspects related to the electronics are, in order of priority:
    a. To show charge signals from the photo-detector;
    b. To perform some level of characterization of the performance of the photo-detector;
    c. To demonstrate the performance of the electronics.

    The group has acquired traces from a high-performance oscilloscope, which show nicely the basic pulse shape and timing performance of the photo-detector itself. An outstanding issue though, is the readout of the custom electronics through the data acquisition system. This measurement appears to be hampered by interference from high voltage pulses associated with the laser used at the APS. The committee recommends that the highest priority for the group be to address the noise problems in the current setup at the APS, and to obtain good measurements for presentation and reviews. Items b and c above will be difficult to present in a satisfactory way without this problem addressed. Alternatively, the group might consider other ways of obtaining these benchmarks that do not involve the use of a noisy laser system.

3. Regarding the noise problem from #2 above, the group might consider the use of isolated power for the front-end system boards as a way to eliminate potential ground loops. Another technique used frequently in front-end electronics is the use of point-of-load regulators to help with the overall power system design.

4. Regarding characterizing the performance of the tile from #2 above, after the noise problem is addressed, the group should focus on the characterization of the performance. This will be important should any deficiencies in some aspects of performance be revealed that might lead to the need for improvements in the tile design. While this is primarily a detector issue, there may be aspects relevant to the design of the electronics, embedded algorithms needed, etc.

5. The committee recognizes that only a few months are left for the conclusion of the current project phase. There was a fair amount of discussion and presentation on the large 4 X 3 tile system, but not so much about the performance of a single 8" tile, although a complete 8" ceramic tile with electronics was passed around for show-and-tell. We recommend that the group prioritize on demonstrating the performance of a single tile, which is a core deliverable of the project. Since there were no results presented on the 8" tile, it was not clear if the full characterization of a single tile had not taken place. In the experience of this committee, debugging small-scale systems first before tackling larger-scale systems can lead to a better understanding of the intrinsic performance and a better understanding of the commissioning process. As an added benefit, it would enable getting devices in the community faster.

6. The current front-end chip, PSEC4, appears to be adequate for this phase of the project. One issue was the apparent non-linearity of the sinusoidal response, but this is probably not a show-stopper if it can be understood. For the next phase of the project, the group should consider the design of a new front-end ASIC. Overcoming the limited commercialization opportunities incurred by using the current chip is a primary goal. This might be solved by porting the design to a national lab or a private company. Negotiating the payment of royalties with the CAD software licensing company is also a possibility, although the long-term outlook for applications should be kept in mind. Another performance aspect for the next version of the chip is the buffer depth. This is a critical parameter, as it has implications for the length of the record, read-out dead time, power consumption, bus capacitance, analog bandwidth, and possibly the overall size of the chip. There will need to be an optimization of buffer depth that is driven by specific applications. One issue that the committee identified as undesirable is the use of single-ended digital signals in the I/O of the chip. For low-noise, high-performance applications, differential signals would be preferable.

7. The group should publish more papers on the electronics (in addition to the detector.) In particular, we recommend:
    a. A paper on the PSEC chip;

b. A paper on the overall electronics system;
c. A paper on the anodes is desirable, but it should include simulations that corroborate the measurements. A good simulation environment would also be very useful for optimizing the physical parameters of the strip line, such as width, pitch, dielectric thickness, the use of different conductors, etc.
d. An instrument paper, describing the overall detector, electronics, and performance. Papers on the chip and the electronics (and the anodes if possible) should come first so that the works can be cited in the instrument paper.