

August 22, 2012

Dear Electronics Group Godparents,

The electronics group wishes to thank the Godparent Committee for their recommendations following the Electronics Godparent Review of July 9, 2012. In this document, we list these recommendations, as stated in the committee's report of July 19, and collect our responses. By doing so, we hope to better document our positions and plans for the future.

Best regards,

Electronics and Integration Group

**[Recommendation:1]** The overall architecture of the readout system is very well conceived for this stage of the project. It is general enough to be useful in studying a number of applications that might have different performance requirements. The variety of interface features and timing options are what is needed right now to get photodetector samples into the hands of potential customers and users. We strongly recommend that this aspect be highlighted in a significant way in future presentations and reviews, as we believe it to be one of the key points of this development. One consequence of generality however is having more features than needed for a specific application (e.g. Ethernet, USB, QSFP fiber, different timing options, etc.). Another is increased power consumption. While these are useful for R&D and this phase of the project, we presume that for the next phase, designing for a specific application will narrow the focus and requirements toward an efficient set of features optimized for that application. This should result in a more compact package design, lower power consumption, etc. We recommend that the group give careful thought to this in preparing for the next phase of the project and proposals, as well as upcoming reviews. In particular, we suggest that this set of electronics not be advertised as one size fits all, since it is clear that improvements in certain areas can be achieved at the expense of others. (For example, a water Cherenkov detector would want 100 pSec timing resolution and low power consumption, but the amount of material in the packaging is not important. For a TOF detector, 1 pSec timing resolution is needed, the power consumption is less important, but the packaging and mass is critical...)

**[Response:1]** We thank the committee for the recommendation and agree wholeheartedly. As we move toward hardware that supports specific applications, we endeavor to find potential users who can supply unique expertise on requirements for both performance and packaging. In particular, results of application-specific simulations provided by such users could provide a powerful tool for us to develop streamlined systems targeted to their system's requirements.

We have been in contact with a number of early adopters who have inquired about getting small systems for test, including:

1. the Argoneut beam test in MCenter at Fermilab for a 3-station TOF system for particle ID;
2. Yau Wah, the US co-spokesman for the KOTO experiment, for precision TOF for rejecting combinatoric photon backgrounds;

3. proponents of small non-cryogenic tracking water Cherenkov counters (Daniel, Annie,...) for HEP, nuclear, and reactor-monitoring neutrino experiments;
4. the UC radiology department for a whole-body TOF-PET scanner and a high-throughput small animal scanner;
5. the STAR collaboration for precision TOF at RHIC.

In addition, J. Incandela has expressed interest in the capabilities of a high-precision TOF system at the Super-LHC to separate vertices at high luminosity.

**[Recommendation:2]** To meet the near-term milestone of the project (i.e. the official end of this phase of the project with the deadline of Sept. 30, 2012), the committee believes that the most important aspects related to the electronics are, in order of priority:

- a. To show charge signals from the photo-detector;
- b. To perform some level of characterization of the performance of the photo-detector;
- c. To demonstrate the performance of the electronics.

The group has acquired traces from a high-performance oscilloscope, which show nicely the basic pulse shape and timing performance of the photo-detector itself. An outstanding issue though, is the readout of the custom electronics through the data acquisition system. This measurement appears to be hampered by interference from high voltage pulses associated with the laser used at the APS. The committee recommends that the highest priority for the group be to address the noise problems in the current setup at the APS, and to obtain good measurements for presentation and reviews. Items b and c above will be difficult to present in a satisfactory way without this problem addressed. Alternatively, the group might consider other ways of obtaining these benchmarks that do not involve the use of a noisy laser system.

**[Response:2]** In the month since the Electronics Godparent Review was held, the APS test group has made significant progress understanding and reducing the noise in the test setup. Through improvements in shielding and ground loop mitigation, we now observe primarily laser-uncorrelated noise on the order of 1-2 mV RMS. Though higher than the inherent custom electronics noise (< 1 mV RMS), this noise level is consistent with test results using the high performance oscilloscope and should be acceptable for data analysis.

The hardware, firmware, and software is in-hand and ready for both a 20-channel DAQ system (for use with the 8-inch vacuum chamber MCP testing) and a 60 channel DAQ (for use with the dual-sided readout Demountable MCP testing). Both systems allow for the self-triggering with respect to the trigger photodiode, which is a required feature given PSEC-4's relatively short buffer depth. The electronics and APS testing groups are working closely to get data from these systems into the existing analysis pipeline. Our plan is to perform characterization of both the electronics and MCPs under test, including the key timing and transverse resolution measurements, in the upcoming weeks.

[**Recommendation:3**] Regarding the noise problem from #2 above, the group might consider the use of isolated power for the front-end system boards as a way to eliminate potential ground loops. Another technique used frequently in front-end electronics is the use of point-of-load regulators to help with the overall power system design.

[**Response:3**] Point-of-load regulation is currently implemented on front-end electronics.

[**Recommendation:4**] Regarding characterizing the performance of the tile from #2 above, after the noise problem is addressed, the group should focus on the characterization of the performance. This will be important should any deficiencies in some aspects of performance be revealed that might lead to the need for improvements in the tile design. While this is primarily a detector issue, there may be aspects relevant to the design of the electronics, embedded algorithms needed, etc.

[**Response:4**] This is the plan.

[**Recommendation:5**] The committee recognizes that only a few months are left for the conclusion of the current project phase. There was a fair amount of discussion and presentation on the large  $4 \times 3$  tile system, but not so much about the performance of a single 8 tile, although a complete 8 ceramic tile with electronics was passed around for show-and-tell. We recommend that the group prioritize on demonstrating the performance of a single tile, which is a core deliverable of the project. Since there were no results presented on the 8 tile, it was not clear if the full characterization of a single tile had not taken place. In the experience of this committee, debugging small-scale systems first before tackling larger-scale systems can lead to a better understanding of the intrinsic performance and a better understanding of the commissioning process. As an added benefit, it would enable getting devices in the community faster.

[**Response:5**] Evaluation of both the  $4 \times 3$  tile system and the single ceramic tile are proceeding in parallel, as planned in the original project proposal. We believe these efforts to be complementary. In particular, the manpower resources utilized on them do not significantly overlap, and experience with each system may provide valuable feedback to the other. As such, we do not believe that effort on the ceramic tile will limit progress on the  $4 \times 3$  system, and vice versa, and we look forward to characterization results of both systems as they become available.

[**Recommendation:6**] The current front-end chip, PSEC4, appears to be adequate for this phase of the project. One issue was the apparent non-linearity of the sinusoidal response, but this is probably not a show-stopper if it can be understood. For the next phase of the project, the group should consider the design of a new front-end ASIC. Overcoming the limited commercialization opportunities incurred by using the current chip is a primary goal. This might be solved by porting the design to a national lab or a private company. Negotiating the payment of royalties with the CAD software licensing company is also a possibility, although the long-term outlook for applications should be kept in mind. Another performance aspect for the next version

of the chip is the buffer depth. This is a critical parameter, as it has implications for the length of the record, read-out dead time, power consumption, bus capacitance, analog bandwidth, and possibly the overall size of the chip. There will need to be an optimization of buffer depth that is driven by specific applications. One issue that the committee identified as undesirable is the use of single-ended digital signals in the I/O of the chip. For low-noise, highperformance applications, differential signals would be preferable.

**[Response:6]** We have spent considerable thought and effort on how to address these challenges, but agree with the committee that it continues to be an issue. Though ASICs developed in Hawaii may meet the performance requirements for buffer depth, they are hampered by their development under an academic license. We are actively searching for a company who is interested in commercializing these sorts of designs, based either on the Hawaii deep buffering ASICs or a modified version of the PSEC-4. In addition, we have previous experience with the DRS4 ASIC, developed by PSI, This ASIC is available commercially, and could be utilized, though the performance trade-offs would require evaluation.

**[Recommendation:7]** The group should publish more papers on the electronics (in addition to the detector.) In particular, we recommend:

- a. A paper on the PSEC chip;
- b. A paper on the overall electronics system;
- c. A paper on the anodes is desirable, but it should include simulations that corroborate the measurements. A good simulation environment would also be very useful for optimizing the physical parameters of the strip line, such as width, pitch, dielectric thickness, the use of different conductors, etc.
- d. An instrument paper, describing the overall detector, electronics, and performance. Papers on the chip and the electronics (and the anodes if possible) should come first so that the works can be cited in the instrument paper.

**[Response:7]** We agree with the committee, and are in the process of preparing these papers. Specifically,

- a. A paper on the PSEC chip is now in preparation. A draft based on the previous version of the ASIC, the PSEC-3, had been prepared and undergone a few rounds of revisions. Since the PSEC-4 addresses all the known problems of the PSEC-3, we no longer believe the PSEC-3 paper to be generally desirable, but effort in its preparation will help to speed that of the PSEC-4 version.
- b. We agree that the electronics system is another key topic for a paper. Since the electronics for the  $4 \times 3$  tile SuperModule system is entirely different from that of the single tile ceramic readout, we recognize the potential for two papers. In each case, it would be ideal if papers on their respective ASICs, the PSEC-4 and IRS2, were published or in submission, so that they can be properly referenced.

- c. An anode paper is currently in the reviewing process. A large effort was conducted over the past three years on anode simulations, but ultimately they are incomplete or incorrect. We do not have sufficient expertise or resources to pursue these simulations further. In order to avoid prolonging the publication of significant progress on anode measurements, we intend to publish without simulation results.
- d. This paper is currently being outlined. As the committee points out, this will likely be the last publication, as it should reference all of those suggested above.