Version 1.3 (Final)
May 20, 2013

LAPPD Electronics and Integration Godparent Review Committee Report and Recommendations

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A godparent review of the LAPPD electronics and integration group was conducted on Saturday, April 6, 2013. This is the first electronics and integration review to be conducted as part of the "LAPPD2" effort, which consists of the second three years of the LAPPD project.

The committee members thank the group for their presentations, and are pleased to see great progress on the electronics, with a PSEC4-based readout already operating on the demountable system at the APS, and IRS2-based readout electronics already fabricated in preparation for the forthcoming 8" ceramic system at SSL. Furthermore, we congratulate the group on the recent submission of papers on the anodes and the PSEC4, and look forward to seeing them in publication.

The following are comments and concerns raised within the committee as the project moves forward into its second phase:

[1] Making a well-documented compact demonstration system for early adopters is an important goal for the electronics/integration group. We recommend that the group carefully consider what the expectations of the proposed early adopters might be, and focus effort on making sure that the system can easily meet these goals. It should be laid out clearly what the system can and cannot do, so that there are no unmet expectations.

[2] Five potential applications were presented as targets for future development. The committee is concerned about the logistics of supporting development on multiple simultaneous fronts, especially given the current limits on available manpower. As such, we recommend strongly that the group focus on one particular application for the immediate future. We recommend the following criteria be used in this selection:

a. The requirements should be well specified.

b. The specifications should generally be achievable with existing electronics. For instance, the system should be based around an existing ASIC, such as the PSEC4 or IRS3B, as opposed to an ASIC that still needs to be designed, like the PSEC5. If it has not already been done, we recommend that the group investigate the possibility of purchasing additional samples of PSEC4 from MOSIS, which may be available from a previous run but not yet diced.

c. The working system should demonstrate some significant improvement over existing technologies.

d. The target user(s) should be enthusiastic about the development, with clear expectations, such that after successful deployment they are expected to become a powerful third party endorsement.

Details of the selection process are of course up to the group, but regardless of the chosen application, we recommend the group prepare more specific documentation on the goals and requirements, along with some justification for the choice and how these specifications will be achieved.

[3] There was some discussion over the choice of the TSMC process versus the IBM process for future ASIC submissions. The benefits of switching to the TSMC process are considerable, with lower potential fabrication cost, more frequent submission cycles, and a generally more reliable turnaround time. The TSMC process has also been selected by CERN as either a replacement or complement for the current IBM 0.13 um process. The main disadvantage to switching to TSMC is the inability to use existing design elements from the PSEC4. As the timeline for the PSEC5 is not tightly constrained, and because the design may be undertaken by those not already familiar with the IBM design rules anyway, there seems to be low risk overall to switching to the TSMC process. The committee recommends that this be the baseline process for future ASICs. Some design studies should be undertaken to see if the process is truly suitable for PSEC5, and the decision can be revisited at the next godparent review.

[4] Though there was some discussion of system synchronization, the committee recommends that a detailed plan be prepared or presented for how synchronization is performed between various boards and ASICs, as this will become essential as the systems grow from the existing prototypes.

[5] Some of the component decisions on existing cards seem to be based on relatively minor money savings, for example a few hundred dollars on FPGA costs. The committee recommends evaluating whether such savings are truly significant or "in the noise." Higher performance FPGAs may make the design work easier, for example, which could save precious time for those working on the system development, as well as allow increased flexibility for future evolution of the system. We encourage continued effort in assessing and developing architectures for the readout system that will be open and adaptable.

[6] As the program moves toward deploying systems in target applications, stable long-term support will be required for these applications. This could be obtained, for example, by bringing national lab or company resources onto the project. Other sources of funding could (continue to) be investigated in order to facilitate these additions.

[7] The list of potential early adopter applications is already quite full. However, for longer term planning purposes, it may be fruitful to develop relationships with potential collabora-

tors in the cosmic frontier, if this can be done without detracting from the immediate need to focus on the first delivered system.

[8] In order to provide a broad impact and potential cost savings to a variety of large experiments that may utilize LAPPD devices, we encourage the ongoing efforts to assess and expand generic features that are broadly desired. Initial electronics may serve as an "evaluation platform" or "demo kit" for other potential users, some of whom may decide to create their own custom readout infrastructures. However, it seems less likely that they will want to fabricate their own custom ASICs. With this in mind, we strongly encourage the group's continuing research into generically desirable features on the PSEC5, including deeper analog memory to enable a longer trigger latency (while maintaining excellent bandwidth demonstrated by the PSEC4), use of internal DACs to provide more flexibility for sampling rates and Wilkinson ADC timing, and other investigations into the trade space involving dynamic range, dead time, and other details of the ASIC trade space.

The committee would like to again thank all the participants for their presentations, comments, and discussions, and we look forward to seeing the first successfully deployed systems in the future.