PSEC4 → PSEC4a

Eric Oberla
Univ. of Chicago
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PSEC4 --- PSEC4a :: overview

<table>
<thead>
<tr>
<th>Parameter</th>
<th>PSEC4</th>
<th>PSEC4a</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channels</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>Sampling Rate</td>
<td>4-15 GSa/s</td>
<td>2-11 GSa/s</td>
</tr>
<tr>
<td>Primary Samples/channel</td>
<td>256</td>
<td>256</td>
</tr>
<tr>
<td>Total Samples/channel</td>
<td>256</td>
<td>1024 (or 2048?)</td>
</tr>
<tr>
<td>Recording Buffer Time at 10 GSa/s</td>
<td>25.6 ns</td>
<td>100 (or 200) ns</td>
</tr>
<tr>
<td>Analog Bandwidth</td>
<td>1.5 GHz</td>
<td></td>
</tr>
<tr>
<td>RMS Voltage Noise</td>
<td>700 μV</td>
<td>~same</td>
</tr>
<tr>
<td>DC RMS Dynamic Range</td>
<td>10.5 bits</td>
<td>~same</td>
</tr>
<tr>
<td>Signal Voltage Range</td>
<td>1 V</td>
<td>~same</td>
</tr>
<tr>
<td>ADC on-chip</td>
<td>yes</td>
<td>~same (+extend linearity)</td>
</tr>
<tr>
<td>ADC Clock Speed</td>
<td>1.4 GHz</td>
<td>yes</td>
</tr>
<tr>
<td>Readout Protocol</td>
<td>12-bit parallel</td>
<td>2 GHz</td>
</tr>
<tr>
<td>Readout Clock Rate</td>
<td>40 MHz</td>
<td>same or 600MHz serial rate</td>
</tr>
<tr>
<td>Average Power Consumption</td>
<td>100 mW</td>
<td>~similar, (higher when ADC running non-stop)</td>
</tr>
<tr>
<td>Core Voltage</td>
<td>1.2 V</td>
<td>same, though option to run analog voltage up to 1.4V for more signal range</td>
</tr>
</tbody>
</table>

Main improvement is the moderate increase in sample length = the ability to **multi-hit buffer events that are close in time**. PSEC4a will be able to sample/digitize/readout simultaneously.  
→ Enables dead-time less operation for a certain experimental event rate (CW+burst)
PSEC4 :: overview/reminder

- 6 channel, 256 samples/channel
- Each channel has a threshold-level discriminator
- Sampling rates up to 15 GSa/s
- Single event buffer
  - Time between events limited by ADC + readout latency
- We designed in early 2011 (!)
  - There have been 3 fabrication runs
  - Other than UC, primary user has been Sandia national lab for digitizing fast, short pulses at their Z-machine. Well defined trigger, low rate
- UC has developed 100-channel systems (OTPC, etc)
- We’ve learned a lot since then…motivation for upgrading the design to PSEC4a
PSEC4 architecture overview/reminder

- PSEC4 architecture makes (1st-order) calibration relatively easy. Nominally same or better for PSEC4a
  - Oversampling signal (>~5x Nyquist) alleviates many issues with time-base calibration. PSEC4 time-step variation is 13% (improved in PSEC4a)

- Each analog cell with a linear, full-range comparator for the on-chip ramp-compare ADC. For 80% of voltage range, smaller than 2% deviation from linearity (similar in PSEC4a). Limited by 1.2V core voltage of 0.13 micron CMOS.
PSEC4 architecture overview/reminder

- PSEC4 architecture makes (1st-order) calibration relatively easy
  - On-chip delay-locked loop keeps sampling rate stable and phased-aligned between different PSEC4 chips. Works best on a low-jitter 40 MHz input clock

Analog DLL pulls `vcdl_clk` to lock on next `ref_clk` edge
When locked, sampling rate given by `clock_frequency * num_stages` ('up-conversion')

Diagrams from Chang, et al; IEEE journal solid state circuits Vol. 37
PSEC4 :: thermal noise limitations

\[ \sqrt{\frac{k_B T}{C}} \] (broadband thermal noise on sampling capacitor)

- Want to minimize sampling capacitor size for analog bandwidth, but can’t be too small for noise reasons.
- PSEC4 – effective sampling capacitance is 20 fF :: thermal noise contributes ~ 0.5 mV (RMS 60 electrons!!)
- This is dominant noise source in PSEC4 (measured ~ 0.7 mV RMS). Ramp-compare ADC least-significant bit set below this level to ensure quantization error is sub-dominant
PSEC4 platforms

- Hardware + (lots of) firmware required for system integration of ASICs. Much work has gone into PSEC4 systems; to a certain degree transferable to PSEC4a

- 6-channel, 1.5 GHz, 10-15 GSa/s evaluation module
- USB readout / powered over USB
- For best results, put in an RF box
- First pulses into PSEC4 from LAPPD MCP
PSEC4 ::platforms

• Hardware + (lots of) firmware required for system integration of ASICs.

- 2x RJ45 connectors for flexible system operation (1 clock + 7 LVDS data lines up to **800 Mbps per line**)
- USB 2.0 for standalone operation
- Calibration pulse input
- 30 channels of PSEC4
- Signal conditioning mezzanine / signal input. Plugs into LAPPDs with ribbon coax cable
- 5V power ~1.5A

A 30-channel 10 GSa/s ‘scope’
PSEC4 :: platforms – the ‘OTPC’

- ~200 channel system, readout over parallel USB links (not the best!), using multi-level trigger system (firmware).
  1) PSEC4 self-triggering capability formed L0 trigger within 20 ns. Analog values frozen on PSEC4 channels.
  2) Beam trigger formed by external NIM logic within 100’s ns.
  3) Coincidence of 2 = digitize and read-out PSEC4’s, otherwise release L0 trigger and re-engage
PSEC4 :: platforms – the ‘OTPC’

- Showering-type event (satisfied thru-going trigger)
- Fit waveforms on each MCP-PMT microstrip line for photon time-of-arrival, longitudinal position, and amplitude (only pedestal subtracted waveform, shown for a single channel):

Particle output tagging

\[
\text{PSEC4 ADC Counts}
\]

\[
\text{Time [ps]}
\]

t0 of waveforms (can tell by discontinuity) – L0 trigger time marginal, but it works
OTPC: the time-projection

Example event – after first-level of data processing along the OTPC z-axis

(1) Each data point is an individually resolved photo-electron
(2) Cherenkov photons are recorded over an event duration of ~2 ns

Typical event (thru-going μ)

~(speed of light)^{-1}
OTPC: the time-projection

Example event – after first-level of data processing

along the OTPC z-axis

Typical event (thru-going μ)

Projecting the direct photons onto the reconstructed r-coordinate at each PM

track x vs. z coordinates

track y vs. z coordinates
PSEC4 -----> PSEC4a

- Fix the primary PSEC4 limitation: sample depth at 10 GSa/s

PSEC4: red = acquired

Though late pulses won’t be fully recorded, PSEC4 self-trigger + FPGA allows the hit times recorded (TDC mode)

PSEC4a: red = acquired
PSEC4a – multi-hit buffering

- How many buffers? Considering 2 options: 1024 or 2048 samples per channel
  - Layout space ($) / number of ADC’s trade-off vs. typical event occupancy/timing characteristics
- Operation modes:
  - **Clocked addressing**: blocks around 40 MHz sample clock. Blocks time-stamped on ASIC
  - Use threshold-trigger to determine which 25-ns blocks to record
  - Allows for continuous waveforms, if desired

- **‘Trigger-and-transfer’**: asynchronous blocks, 25 ns wide. (PSEC4-like operation, w/ multi-buffer)
  - Use threshold-trigger to determine which 25-ns blocks to record. Failsafe mode that bypasses on-chip timing block
PSEC4a

- How many buffers? Considering 2 options: 1024 or 2048 samples per channel
  - Layout space ($) / number of ADC’s trade-off vs. typical event: occupancy/timing characteristics

  How does this translate into time and occupancy per channel?
  How large does your ‘effective sampling depth’ need to be per-event per-channel?

  ![Graph from Caravaca et al.](image)

  Low occupancy in the tail region. The PSEC4a strategy would be to record only small time-windows (~25 ns) around actual signals in this region, as determined by a self- or external-trigger (vs. continuously recording mostly baseline).

My strategy would be (per-channel at 10 GSa/s):
- With a 1024 sample buffer: always record first 50 ns, leave two 25 ns buffers for late hits
- With a 2048 sample buffer: record first 100 ns, leave two (four) 50 ns (25 ns) buffers for late hits
  - The 2048 buffer option might be preferable?
  - 2048 is likely the absolute maximum depth to keep PSEC4-like architecture, though feasibility needs to be investigated. 1024 cells is definitely doable, a first layout is done!
How large does your ‘effective sampling depth’ need to be per-event per-channel?

Instead of capturing the full 400 ns or 1 µs waveforms, the PSEC4a design is targeted to record regions-of-interest within this frame.

Initial PSEC4a plan was 4x PSEC4 (1024 samples). 2048 samples might be possible. Waveforms recorded in blocks of 256 samples which are ~25 ns long at 10 GSa/s operation

For randomized signals, 1024 is probably sufficient. For scintillator-based experiments, signals are correlated in time. Given a typical event occupancy, we should be able to determine efficiency of PSEC4a in a certain application [or, conversely, specify PSEC4a requirements based on expected occupancies and minimum efficiency.]

Let’s discuss today ...this really is the key question
PSEC4a – design status

Spent ~3 weeks in September trying various architectures for the primary--> storage sample transfer. Found a working design solution.

Layout for 4 cells on right (for the 1024 sample-depth version, ~50x250 sq. microns). Won’t be the final version.

Now, maximally a part-time effort. A long-ish list of things to simulate/layout. Shorter list of items to put into schematic form.

Given full specs (and welcomed help, particularly running simulations), could be fairly fast to finishing (~months). Re-using many blocks from PSEC4.
PSEC4a – design status – integrated comparator for ADC

Plot shows linear comparator response - keeps good linearity from PSEC4.

- Potentially extended linearity and signal voltage range by increasing analog vdd (increased power draw, potential issues with stability over time – IC process guide sets upper limit at 1.5V power supply operation)
- 1 V linear at nominal 1.2V core voltage. Signal pedestal (offset) level can be set off-chip
- Sacrifice some careful layout/transistor multiplicity to fit in PSEC4a – cell-to-cell matching probably won’t be as good
Main control lines shown. (Not all I/O’s). The address to the analog block of 256 cells to which to transfer is specified by the FPGA, registered on-chip.
New blocks, may not make the final cut: not necessary for overall functionality, but very helpful for system integration!
Could imagine a similar architecture used for the PSEC4 readout:
• Digitizer card with PSEC4(a). PSEC4 version has 30 channels.
• Central system card (clock distribution, interfacing to PC)
• Gigabit serial link / clock / slow control between the 2 cards over CAT5 cable

A new version of a central card has been designed for the WATCHMAN experiment – first use with the ANNIE experiment @ FNAL. (Mircea Bogdan, UC electronics design)

Boards recently fabricated: a reasonable, generic back-end for 1000’s channel-scale PSEC4(a) readout (with current system, each board handles 240 channels PSEC4)
Data collected into Crate Master (ACM) via daisy chained SFPs
- Max Rate inside chain: 6Gbps
- Data Processing/Reduction possible inside ACM
- Final Data readout only from ACM (SFP, CAT5, USB, or VME) or parallel through Gigabit Ethernet -- some firmware work required!
**summary**

- PSEC4a design started – multi-hit buffer version of the 10 GSa/s PSEC4 with 1024, or possibly 2048 samples/channel. The most useful operation mode would be using these samples in discrete 25 ns (at 10 GHz) blocks for buffering multiple events
  - How many samples/channel are needed for these applications, given expected occupancy?
  - Time, priorities, need, and funding determine if we see design to fabrication

- Reusing many of PSEC4’s working parts – and sticking with the well known IBM-now-GlobalFoundries 0.13 micron CMOS process.
- Back-end systems for PSEC4 exist – may be used for large-scale PSEC4a systems as well. A DAQ hardware framework exists. A number of other hardware/firmware entities exist already.

Essential to work collaboratively on this project. A working PSEC4a chip would only be the first step:

- Firmware, software, and a bit of hardware would need developing. We don’t have the person-power or bandwidth to make a generic PSEC4a DAQ system with infinite programmability.
  - A lot exists, but a lot will be specific to experimental needs. Trigger, rates, event-handling, etc.
  - If the chip design fits needs, and if there are people willing to support the investment in the longer term, I think it would be worth the effort.
Back-up: Berkeley specifications for Theia R&D
Table 1: Summary of technical requirements outlined in the document. Voltage resolutions specify the required number of bits per sample for 2V dynamic range. The timestamp would either be reported along with an offset in samples to the trigger from a particular value of the clock if the timestamp has worse resolution than the sample clock or latched at the trigger if the resolution is the same or better than the sample clock. Rollover is given in bits assuming a 100MHz timestamp. Buffer size is given in samples assuming 10 GHz sample clock. Additional non-numeric desires are specified in the document.
Berkeley specs:

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<td>10 GHz (0.1 ns)</td>
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<tr>
<td>Dynamic Range</td>
<td>1 V (fully negative)</td>
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</tr>
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Specs PSEC4a (and PSEC4) fulfill natively. RMS noise level somewhere in between 0.5 and 1 mV
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PSEC4a planned for 100 ns (1000 samples), possibly extended to 200 ns (2000 samples). Not planning to meet this spec for continuous recording – though what is the effective buffer size requirement? See slides 15-16. The basic idea is to only record useful information in the analog buffers, then concatenate data to form event using timestamp info

[n.b.: PSEC4a would meet 400 ns requirement at 5 GSa/s, 2048 samples]
Berkeley specs:

Can extend voltage range by putting variable attenuator in-line with the signal. (Some cost in resolution) This would be done at the board-level, not chip-level. The offset (pedestal) voltage level is also set at the board-level.

The on-chip voltage range limited by core voltage of process (1.2 V). Multi-voltage level designs on-chip beyond the scope of PSEC4a.
Berkeley specs:

Planning on putting a 16-bit rolling timestamp on-chip (clocked at 40 or 80 MHz) to sync pulses in close time proximity (<1 us).
For longer rollover times, these requirements are easily fulfilled in FPGA.
Could be put on chip, would tag the trigger time in the ‘trigger-and-transfer’ mode. Would effectively be a fine time-stamp within each coarse 40 MHz system timestamp. This feature loses functionality when using the default ‘clocked-transfer’ mode. In this mode, it is simple to pick a digital threshold in the FPGA, pick off pulse time with respect to sample
Back-up OTPC slides
In simplest case, track parameters can be solved analytically through ray tracing (ignoring dispersion and scattering).

The time projection of the direct Cherenkov photons on the OTPC z-axis is a measure of the Cherenkov angle ($\beta$) and the particle angle with respect to the OTPC longitudinal axis.

\[
\Delta t_{\gamma 21} = t_o \left(1 - \frac{\beta c}{<v_{group}>} \tan \theta_i\right)
\]

\[
\Delta z_{\gamma 21} = \beta c t_o \cos \theta_i
\]

\[
\frac{dt}{dz} \approx \frac{1}{\beta c} - \frac{\tan \theta_i}{<v_{group}>}
\]
In simplest case, track parameters can be solved analytically through ray tracing (ignoring dispersion and scattering).

Time-resolving the direct and reflected photons provides the lateral particle displacement from the OTPC center-line as a function of $z$- and $\phi$-position.
OTPC Photodetector Module

- 1024 anode pad mapped to thirty-two 50Ω micro-strips with custom anode card
- MCP-PMT mounted to anode card with low-temperature Ag epoxy
- Terminate one end of micro-strip, other end open (high-impedance):

Expressions for the position and time-of-arrival of the detected photon:

\[
x = v_{\text{prop}} \frac{t_2 - t_1}{2} - \frac{D + 2C_1}{2}
\]

\[
t_0 = \frac{t_2 + t_1}{2} - \frac{1}{v_{\text{prop}}} (D + C_2 + C_1)
\]
OTPC Photodetector Module (PM) single p.e.

- Single photo-electron signal recorded by the PM
- 30 channels of 10.24 GSa/s waveform sampling per PM
- Pulses are ~1 ns wide; two pulses on the microstrip anode per photo-electron signal
Scan the laser spot to measure the propagation velocity on the anode microstrip (n.b. similar to prior LAPPD glass anode response, this module has an FR4 substrate)

Measure timing at each beam spot

Timing vs. beam position

- Measure a single-channel timing resolution of 35 ps. (The PSEC4 digitized data are not fully calibrated in voltage and timing)
- The microstrip signal propagation velocity is found to be 0.47 c. Corresponds to a substrate dielectric constant of 4.5, which agrees with the expected value
- Position resolution along microstrip is 3 mm
**OTPC Photodetector Module (PM) multi-p.e.**

- **405 nm pulsed laser**
- **Iris ~1 mm**
- **Filter**
- **lens**
- **OTPC PM**

Pulsed laser (33 ps FWHM) attenuated to multi-photon level + lens

- Measure relative timing between 2 photoelectrons within same laser pulse, which are spatially separated on the MCP-PMT.
- Single photon time resolution is 75 ps.

PSEC4 digitized waveforms + rising edge fits to extract the photon time-of-arrival

- Channel 10
- Channel 21

**Graph:**

- Time difference between 2 photons (ns)
- Entries per 70 ps
- $\sigma_{\text{measured}} = 0.105 \text{ ns}$
- $\sigma^2_{\text{measured}} = (2\sigma^2_{\text{p.e.}} + \sigma^2_{\text{laser}})$
Reconstructed 2D coordinates over MCP-PMT active area

One-sigma statistical errors on the photon transverse position, longitudinal position, and time-of-arrival \((x,y,t) = (2\text{ mm}, 3\text{ mm}, 75\text{ ps})\)

First cosmic ray muon, seen by a single OTPC photodetector module!
Using position-corrected time, remove contributions to the time-projection from the particle velocity (assume β=1)

\[ t'_i = t_i - \frac{z_i}{c} \]

\[ \frac{dt'}{dz} = \frac{dt}{dz} - \frac{1}{c} = \frac{\tan \theta}{<v_{group}>} \]

770 ps

Direct and mirror-reflected Cherenkov photons are clearly separated. We collect more reflected than direct.
Combining the data along the normal and stereo view PMs, we measure an average relative timing between the direct and mirror-reflected photons per event:

59 ps timing resolution → 10 mm spatial resolution

86 ps timing resolution → 14 mm spatial resolution

Measure the average number of photons along the track:
[Preliminary] Muon vs showering-electron ID. Cut events based on signal (charge) deposited in the OTPC rear MCP-PMT trigger

Peak distribution from typical thru-going muons (or non-showering electrons)

Cut peak events from sample, keep others (which may be events with an EM showering component)
Strong correlation between the events cut from the OTPC trigger and the measured number of photo-electrons along the track in the water volume.

[To do a better job, really need a larger detector (more containment), more photodetector coverage, more instrumentation on the beam, and a lower-energy beam ~GeV]
Design challenge 1: analog bandwidth

- Goal to preserve rise-times of fast (photo)detectors while coupling into the chip (= extract best time measurement)
- Bandwidth limited by parasitic input capacitance ($C_{in}$), which drops the input impedance at high frequencies:

$$|Z_{in}| = \frac{R_{term}}{\sqrt{1 + \omega^2 R_{term} C_{in}}}$$

$$f_{3dB} = \frac{1}{2\pi R_{term} C_{in}}$$

$C_{in} \approx 2 \text{pF}$

$R_{term} = 50 \Omega$

$\text{bandwidth} \approx 1.5 \text{GHz}$

1.6 GHz BW