PSEC5 Technical Review

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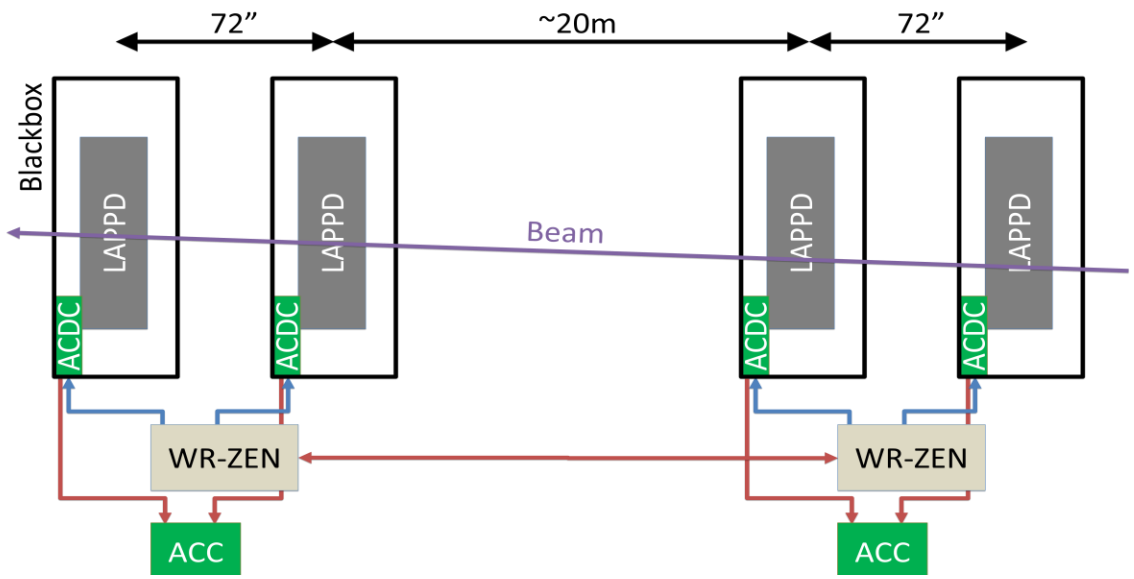
Introduction

Process	65 nm TSMC
Signal to Noise Ratio	1000
Sampling Rate	40 GS/s(5 GS/s)
Buffer Length	6.4 ns(204.8 ns)
Analog Bandwidth	4 GHz
Channels	8
Area	2.4 mm^2



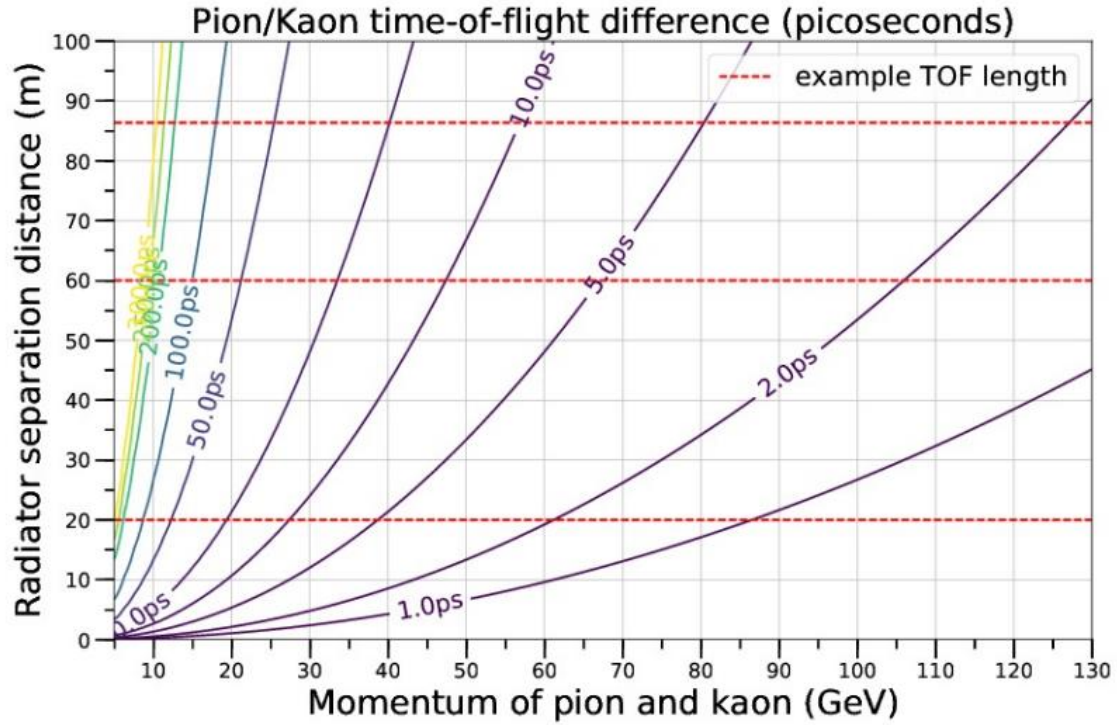
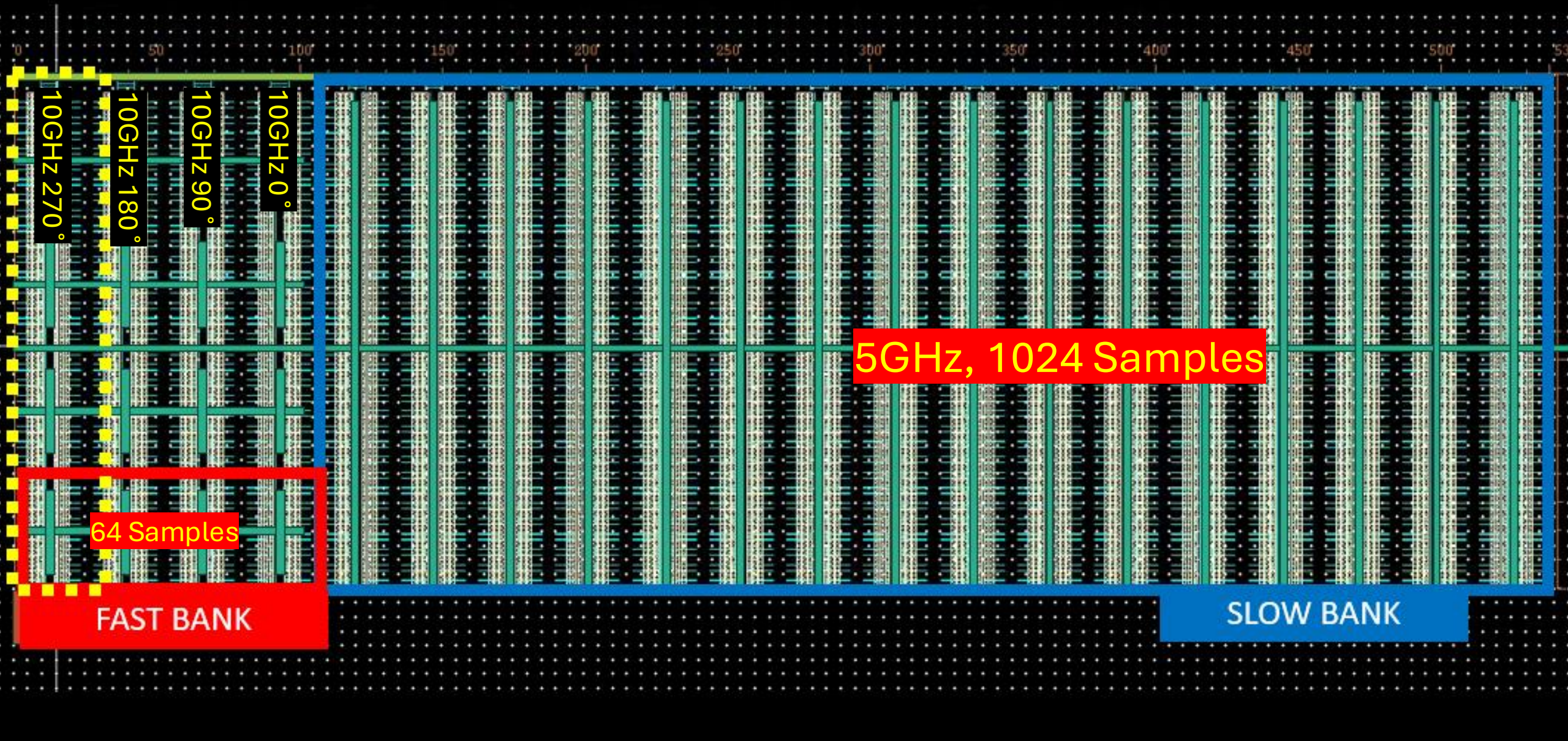
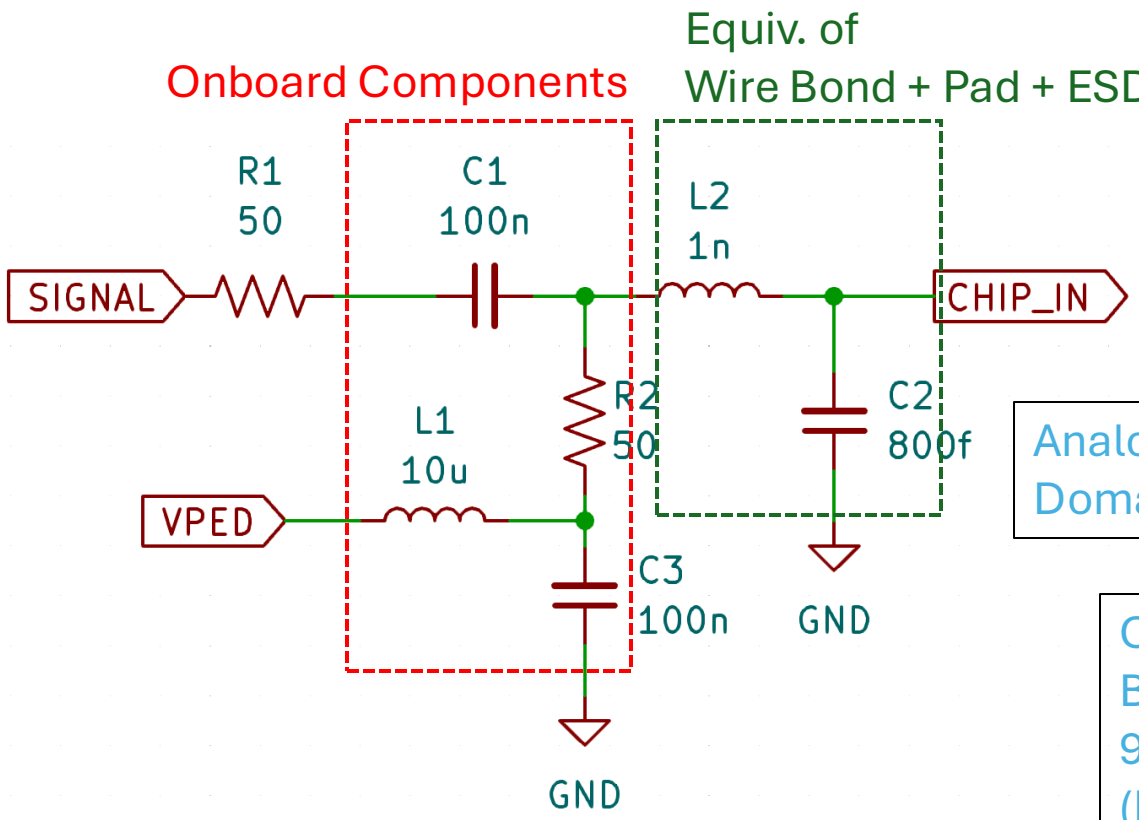


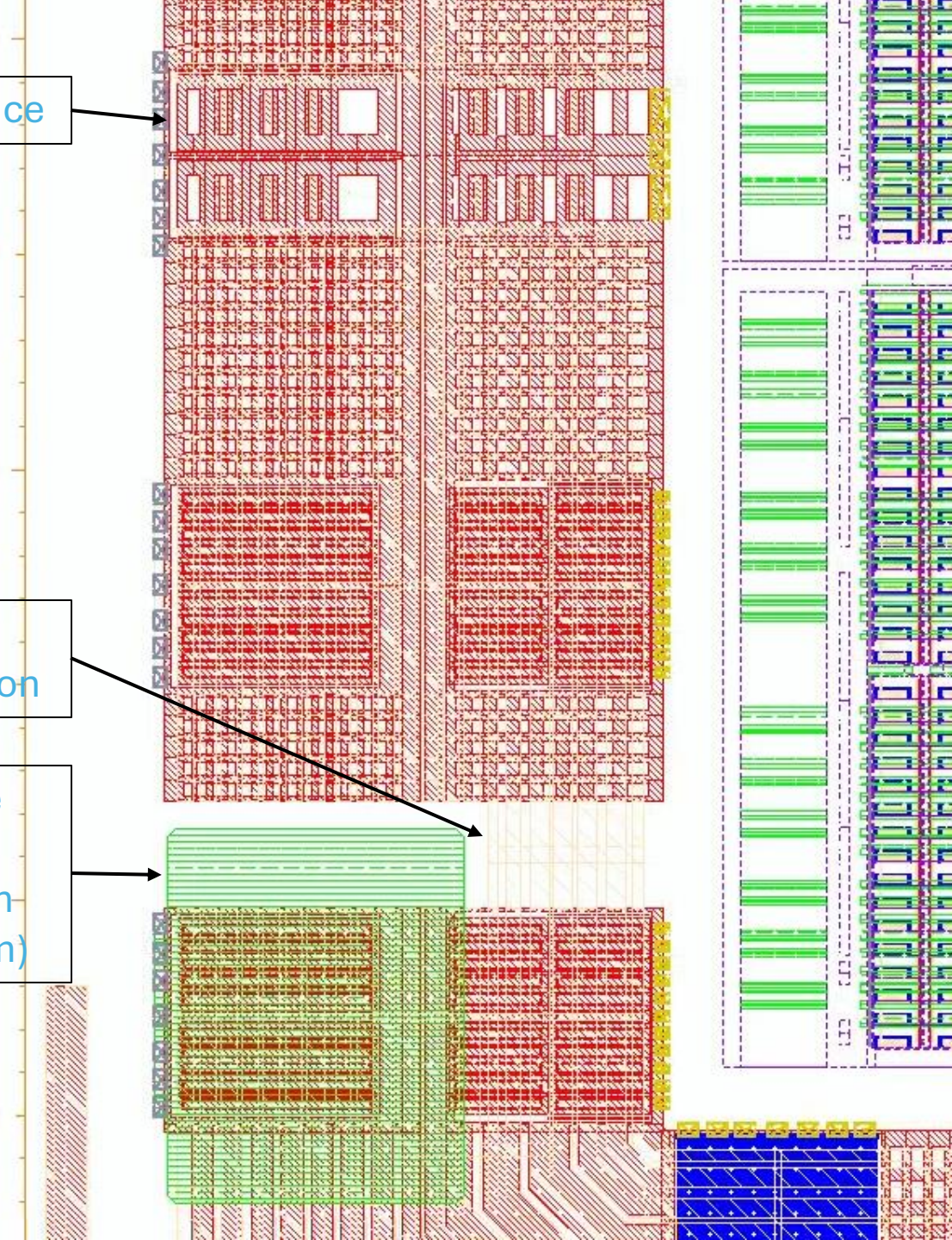
Table of Contents

Single Channel Overview



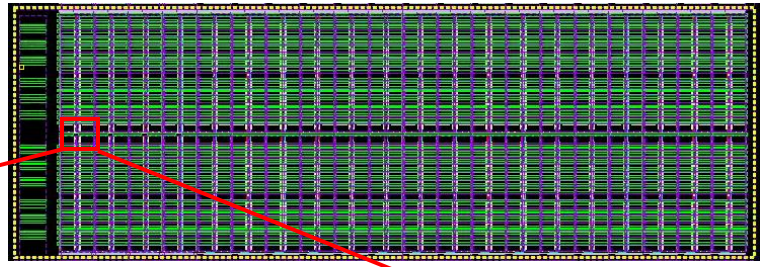
2. Signal Entry

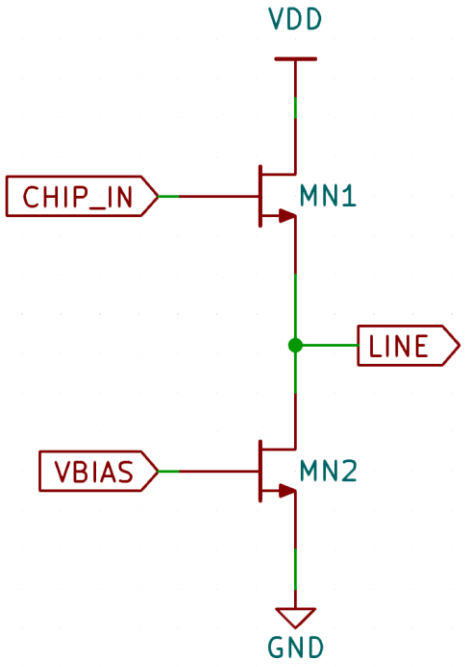


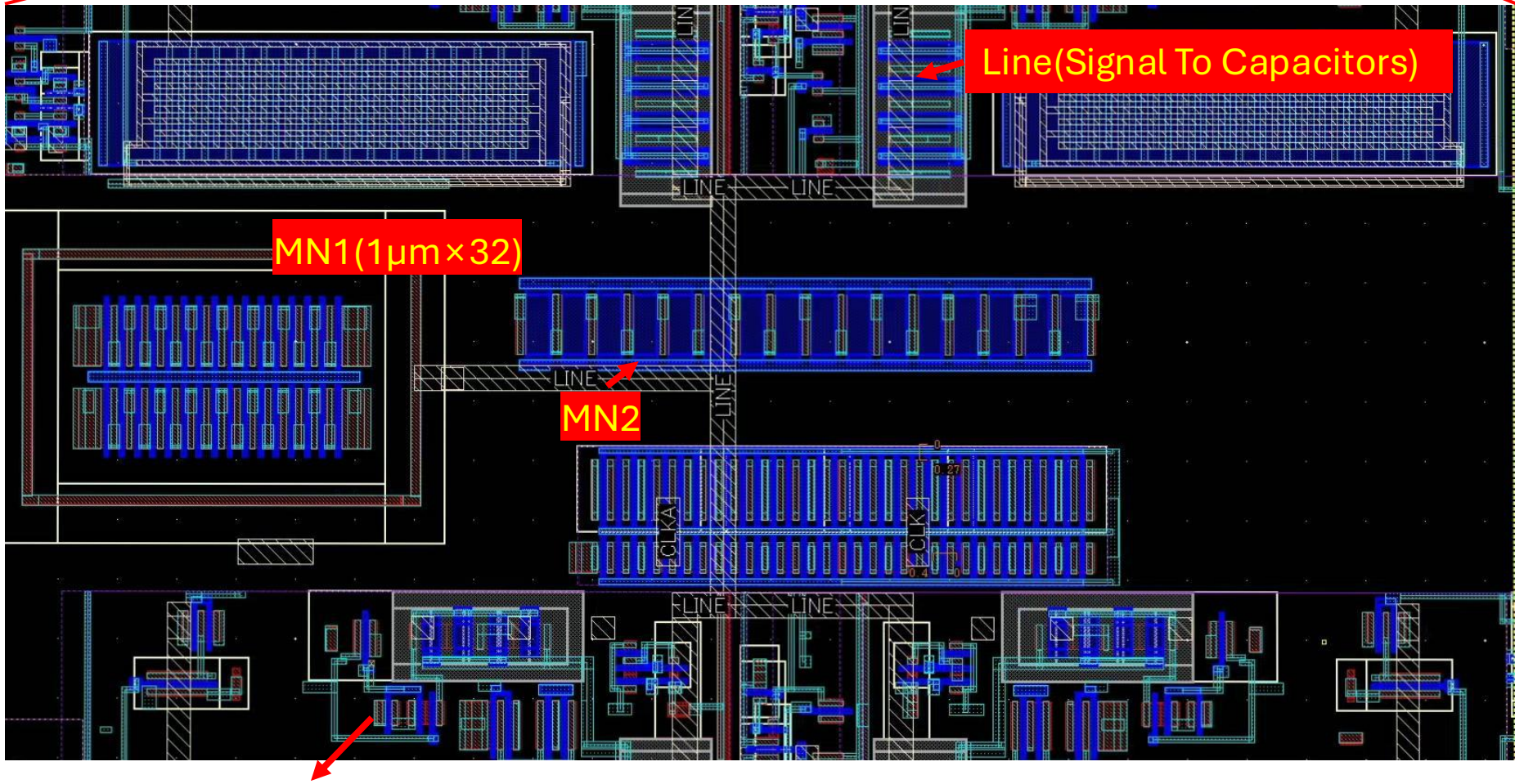


3. Input Source Follower

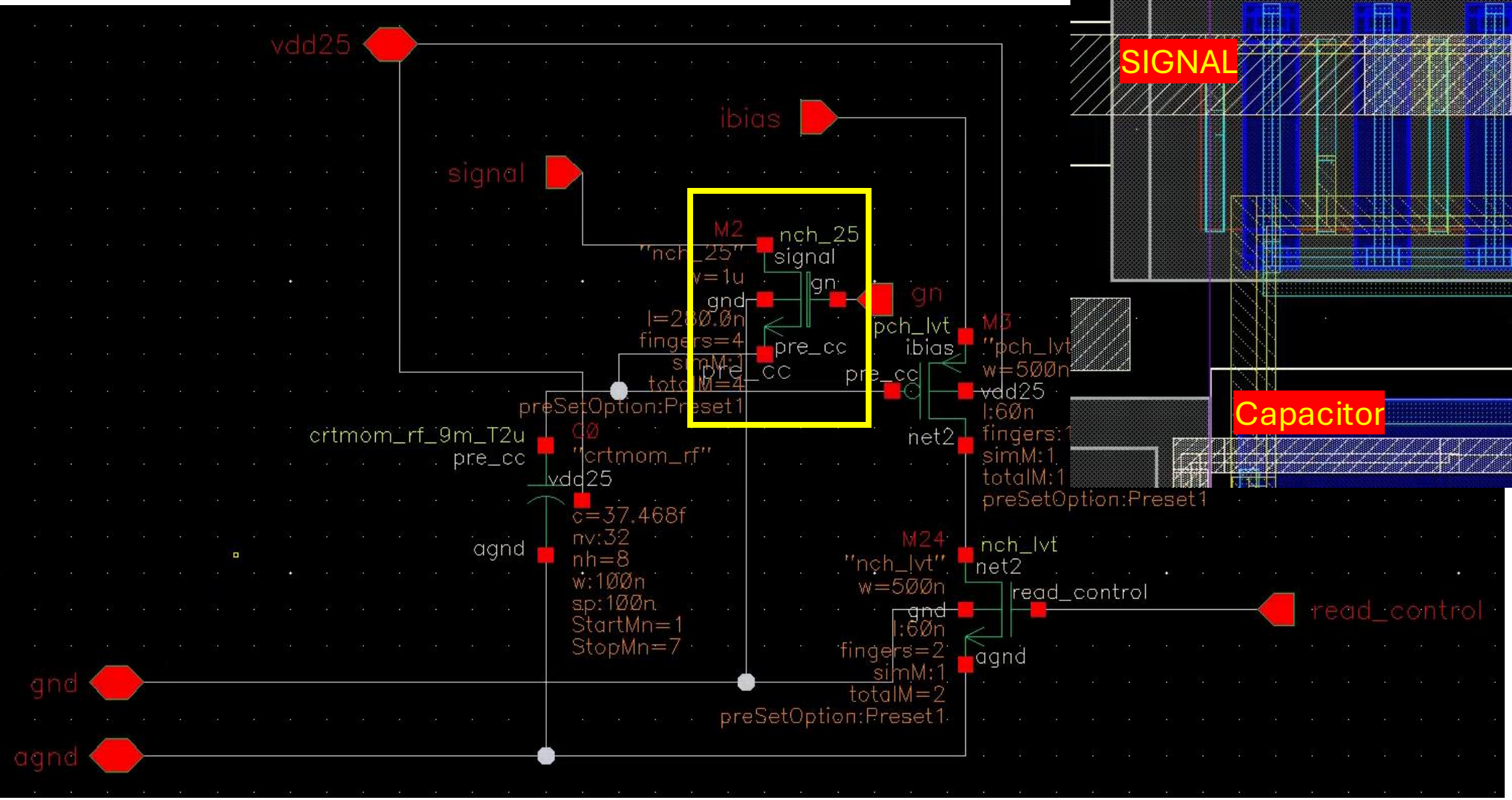
- 5 source followers
- 4 for each fast SCA column(4GHz BW), 1 for the slow SCA bank(1.5GHz BW)







3. Sampling Switch



3. Sampling Switch

	Cmos	Cmos-2.5v	Cmos-lvt	Nmos	Nmos-2.5v	Nmos-lvt	Nmos-hvt
V Range	1.2v	2.5v	1.2v	<1.2v*	<2.5v*	<1.2v*	<1.2v*
Cutoff Freq**	0.6GHz	3.4GHz	2.3GHz	1GHz	6GHz	3.4GHz	<0.1GHz
Length	60n	280n	60n	60n	280n	60n	60n
Hold Time****	68ns	>10us	1.7ns	71ns	>20us	2.6ns	2us

*Higher impedance as the signal voltage reaches vdd, noticeable at V>0.6vdd

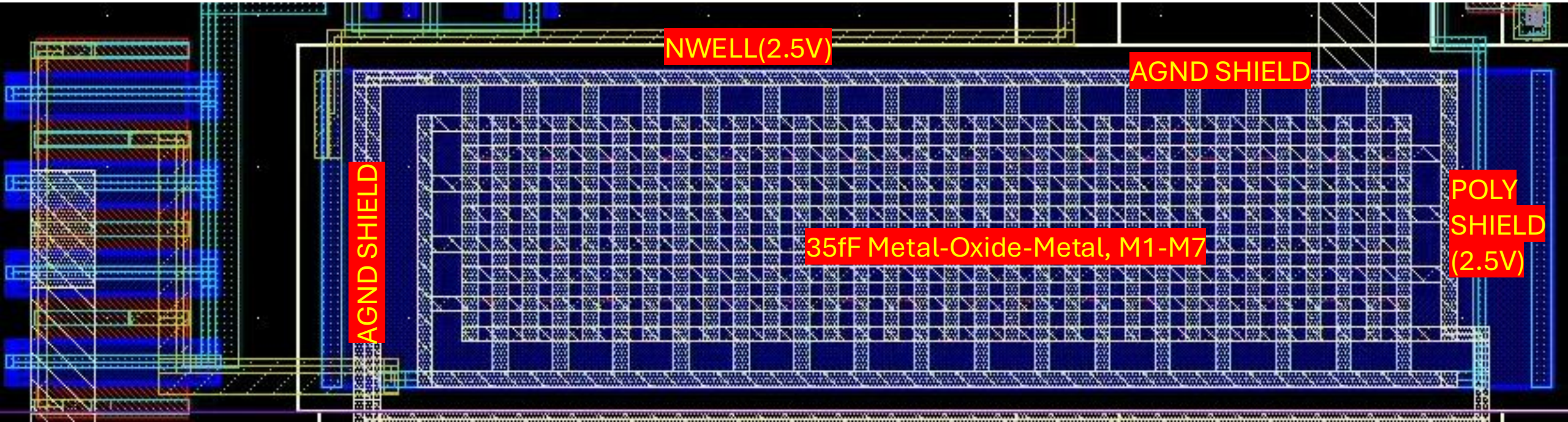
**(Capacitor V Amplitude / Signal V Amplitude) reaches 0.7. ss corner, 0.1V amplitude , DC bias = 0.5vdd

****ff corner, 10% decay after sampling vdd.

4. Sampling Capacitor

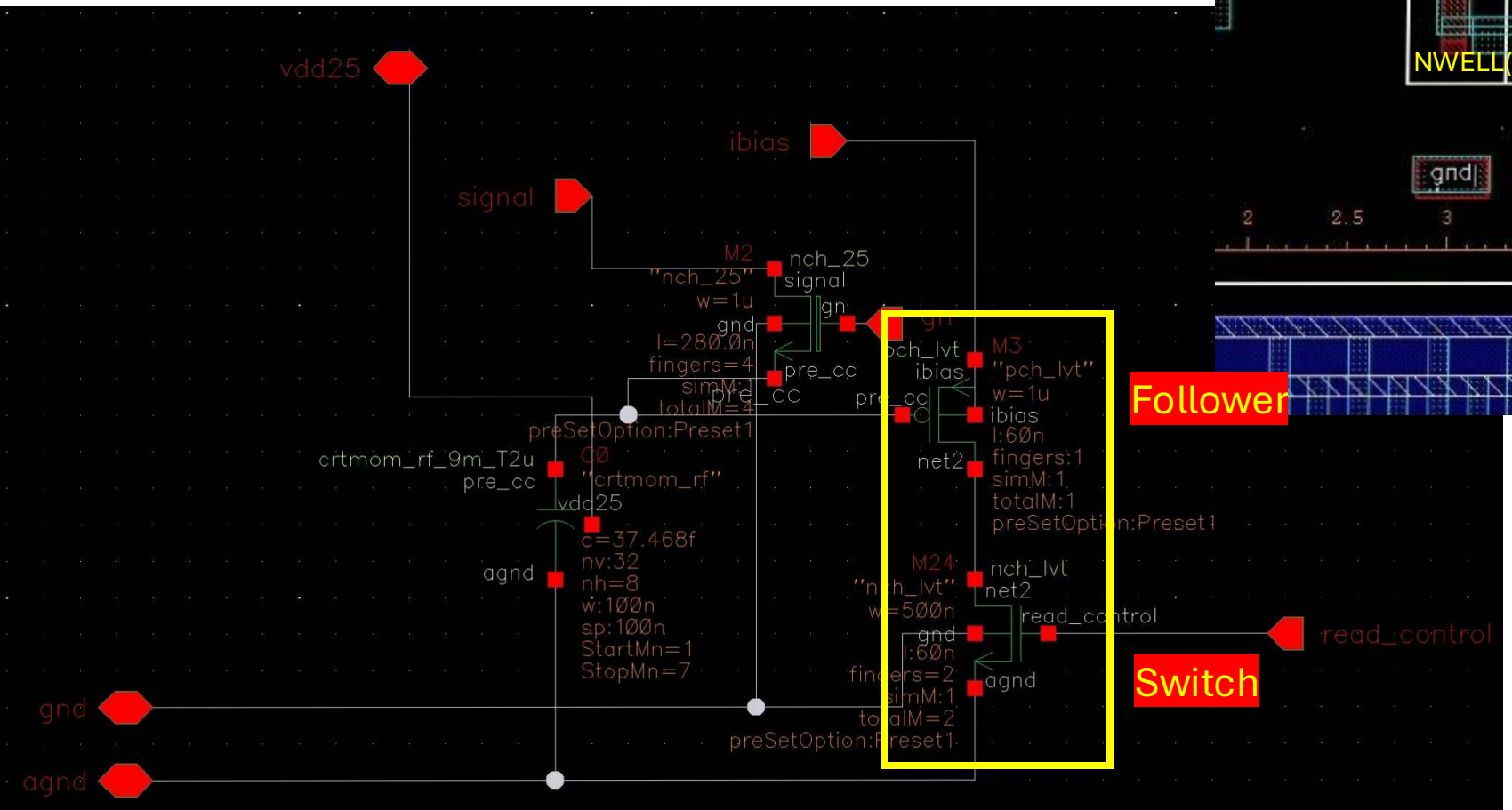
Noise of capacitors at 300 K

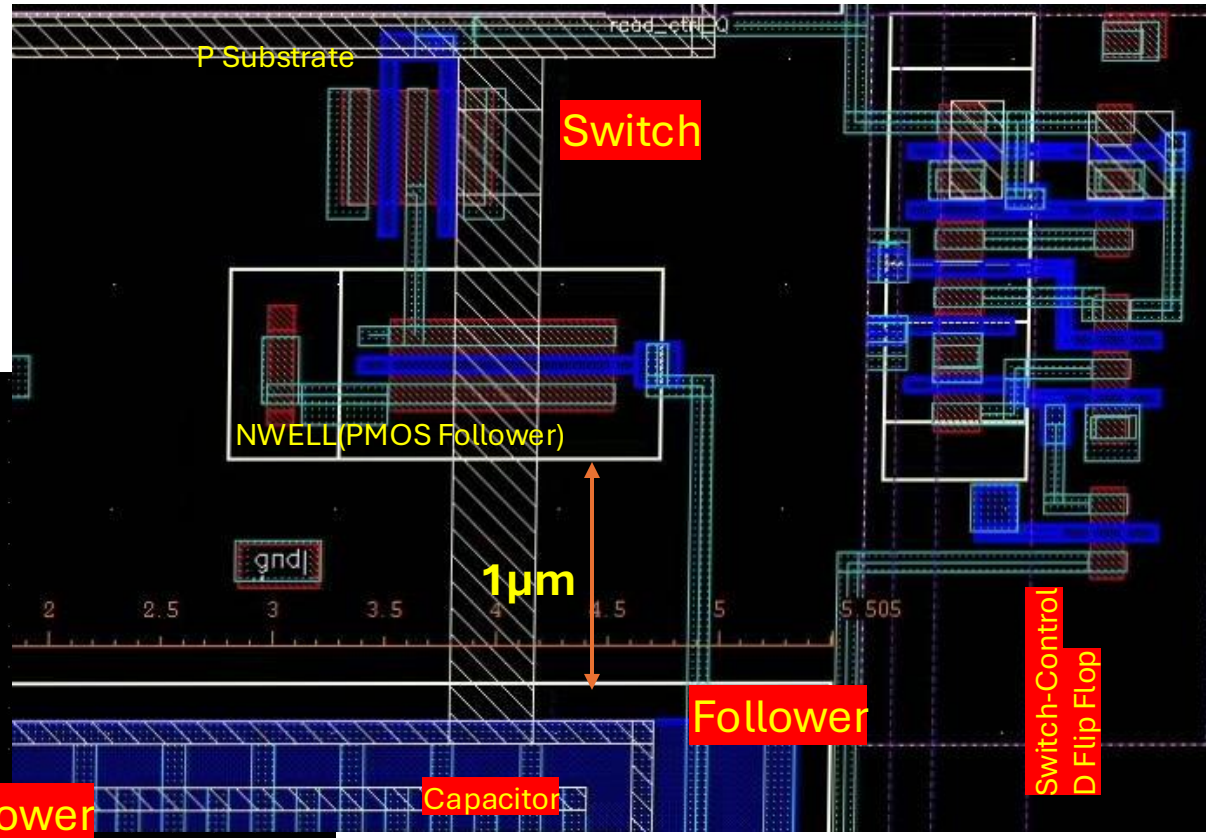
Capacitance	$\sqrt{k_B T/C}$	$\sqrt{k_B T C}$	Electrons
1 fF	2 mV	2 aC	12.5 e^-
10 fF	640 µV	6.4 aC	40 e^-
100 fF	200 µV	20 aC	125 e^-
1 pF	64 µV	64 aC	400 e^-
10 pF	20 µV	200 aC	1250 e^-
100 pF	6.4 µV	640 aC	4000 e^-
1 nF	2 µV	2 fC	12500 e^-

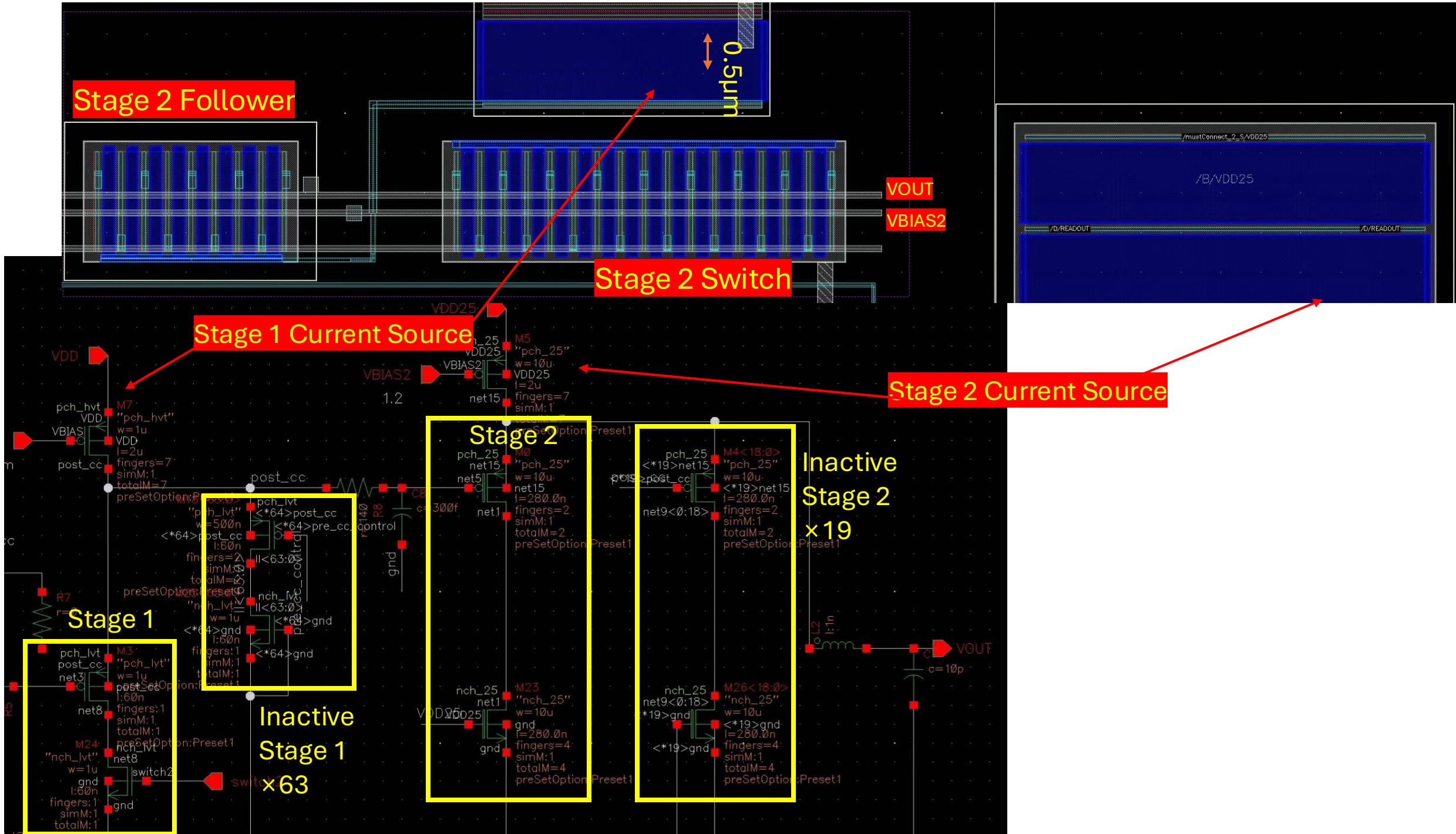


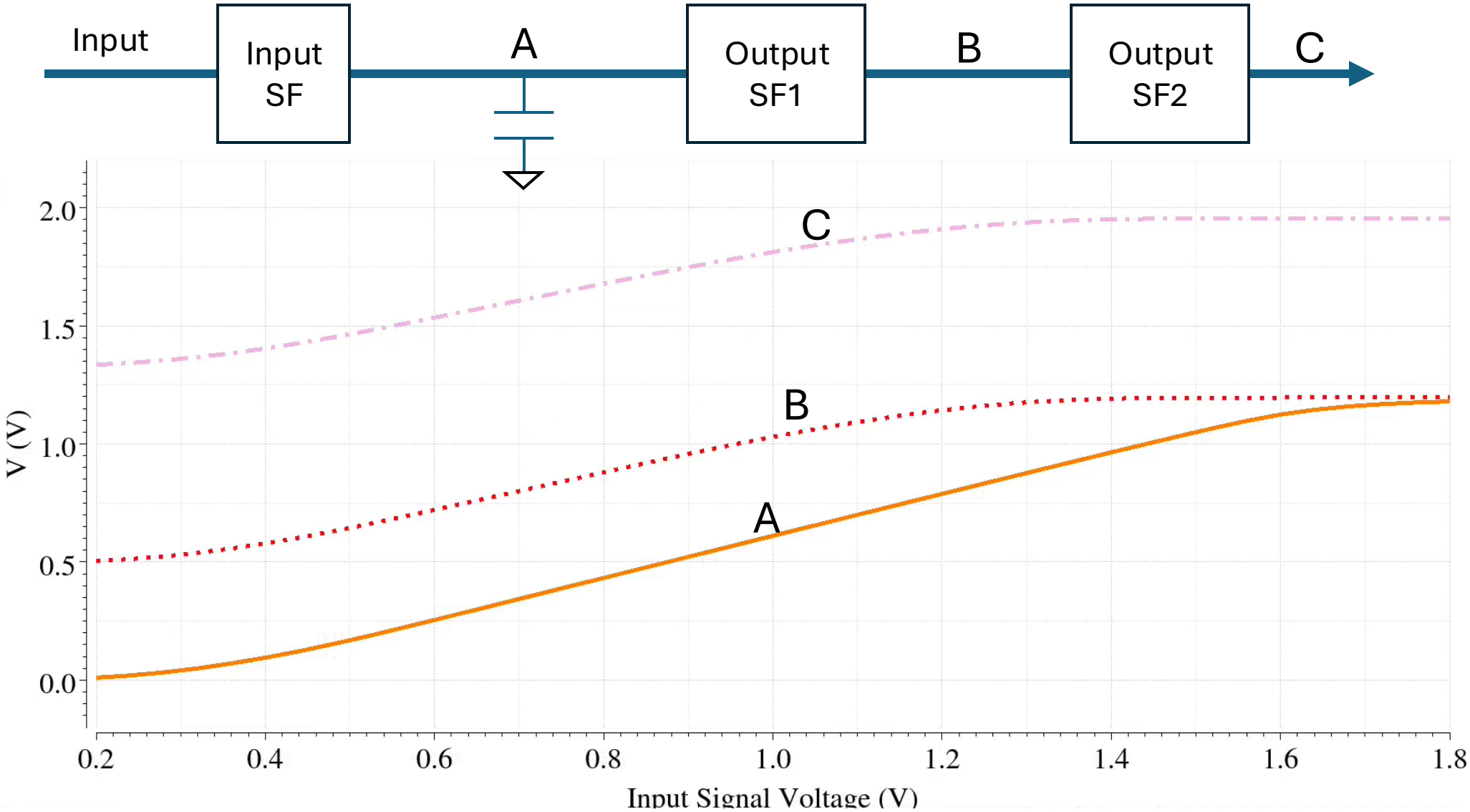
5. Output Source Followers

A. Stage 1



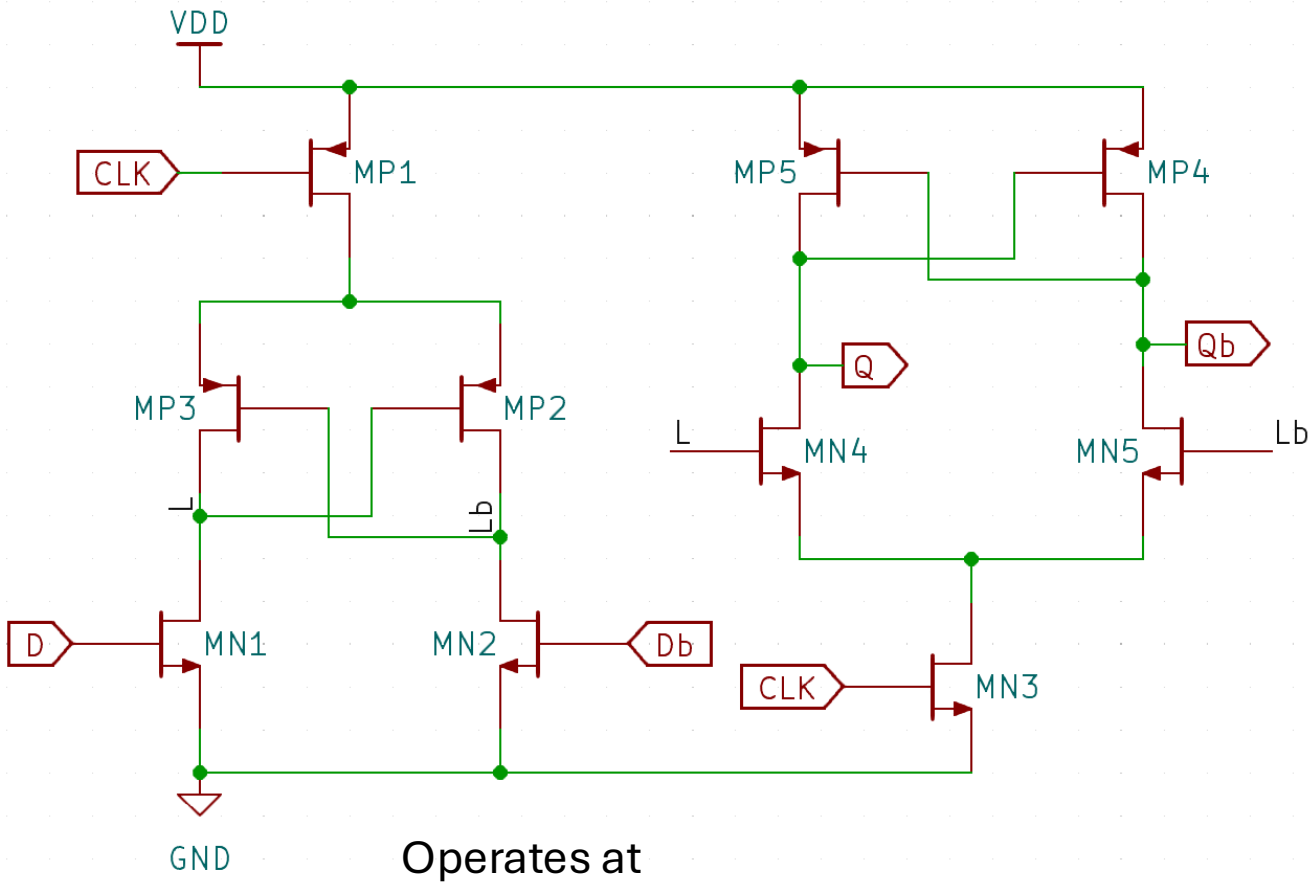



Stage 2 Follower
0.5um
VOUT
VBIAS2
Stage 2 Switch
Stage 1 Current Source
Stage 2 Current Source
Stage 2
Stage 1
Inactive
Stage 1
×63
Inactive
Stage 2
×19
VDD
VBIAS
VBIAS2
VDD25
post_cc
gnd
VOUT
/B/VDD25
/D/READOUT

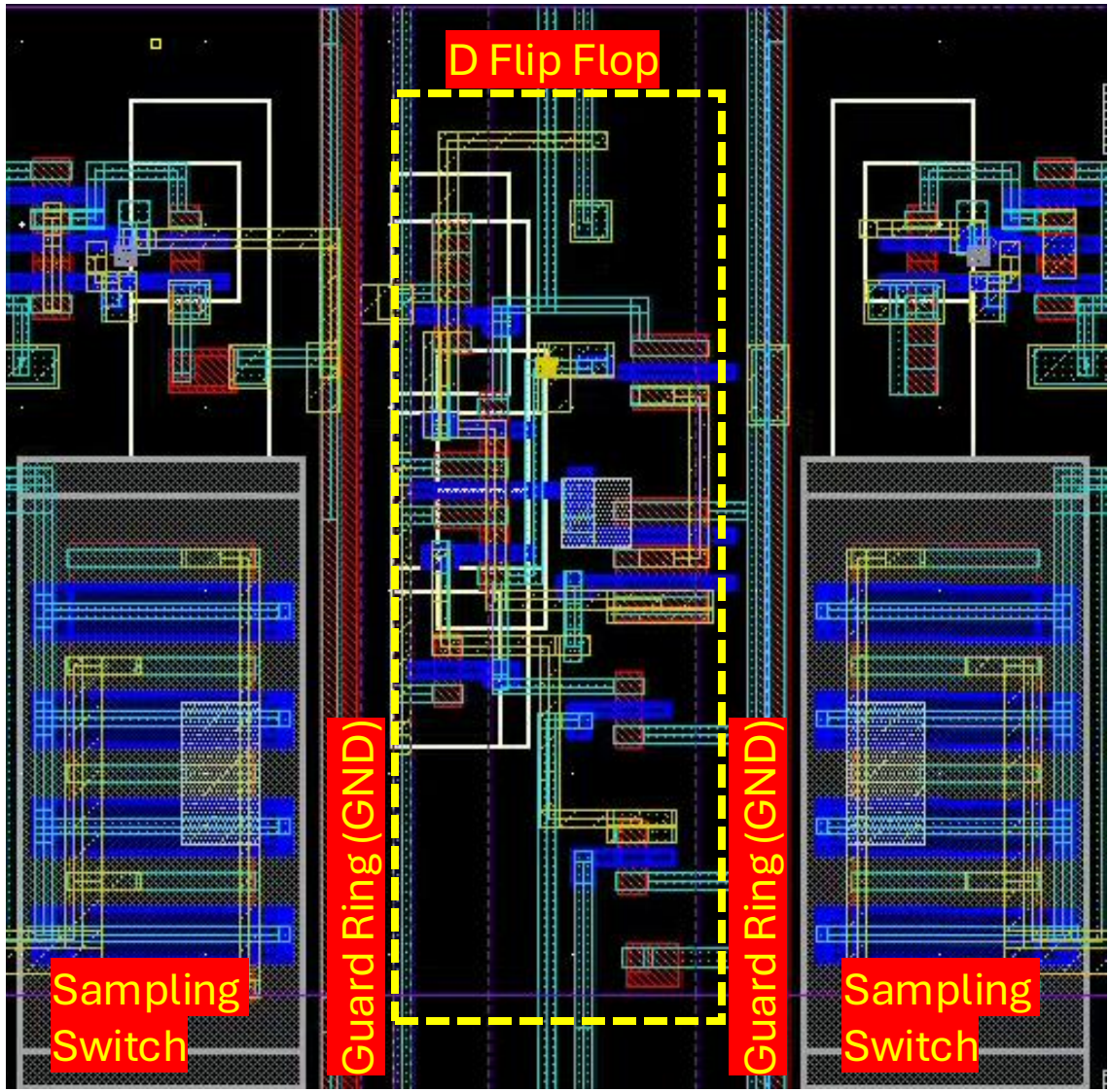

Input
Input SF
A
Output SF1
B
Output SF2
C
C
B
A
V (V)
2.0
1.5
1.0
0.5
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
Input Signal Voltage (V)

6. Controlling Sampling Switch

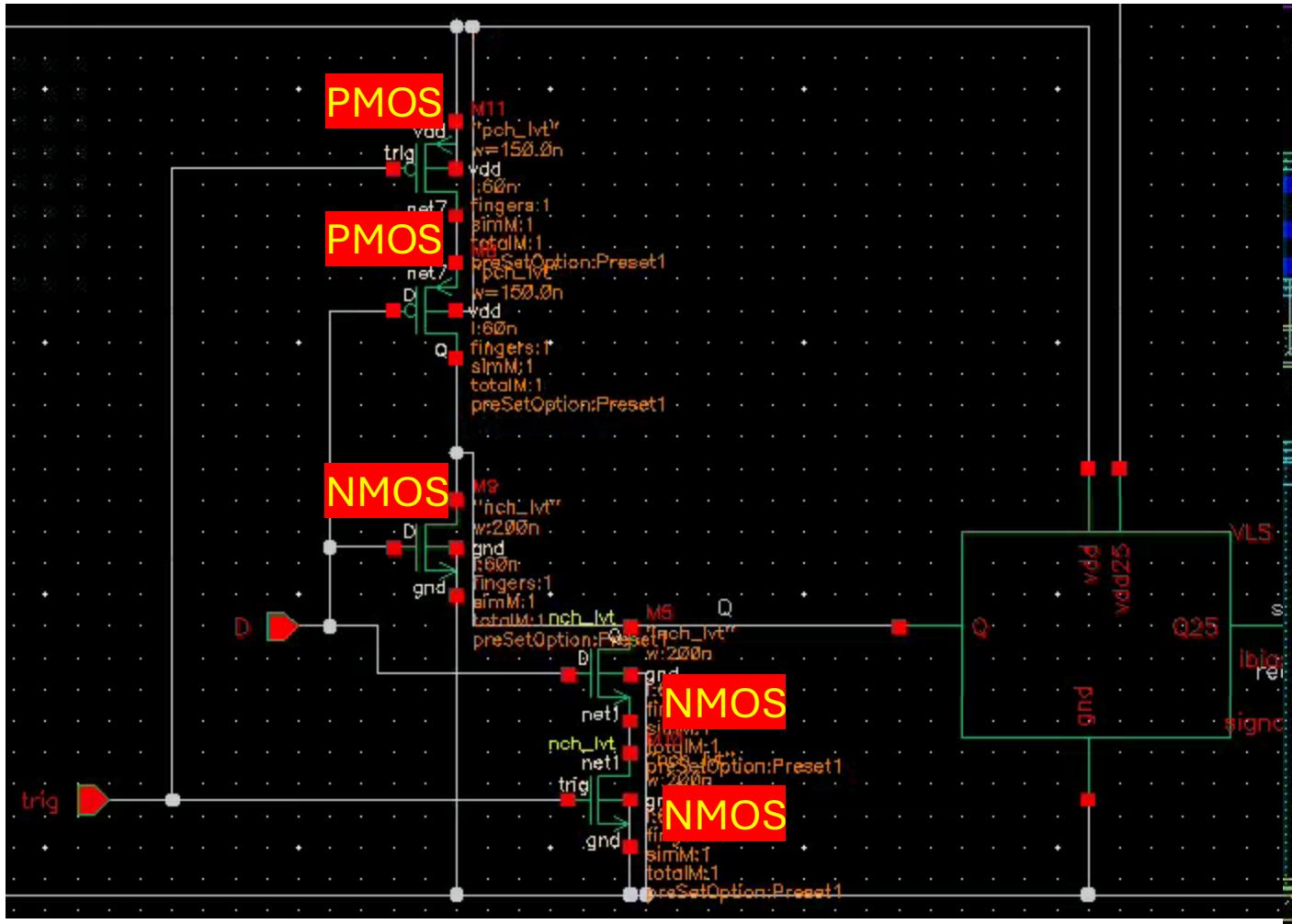
- Dual Edge Triggered Flip Flop

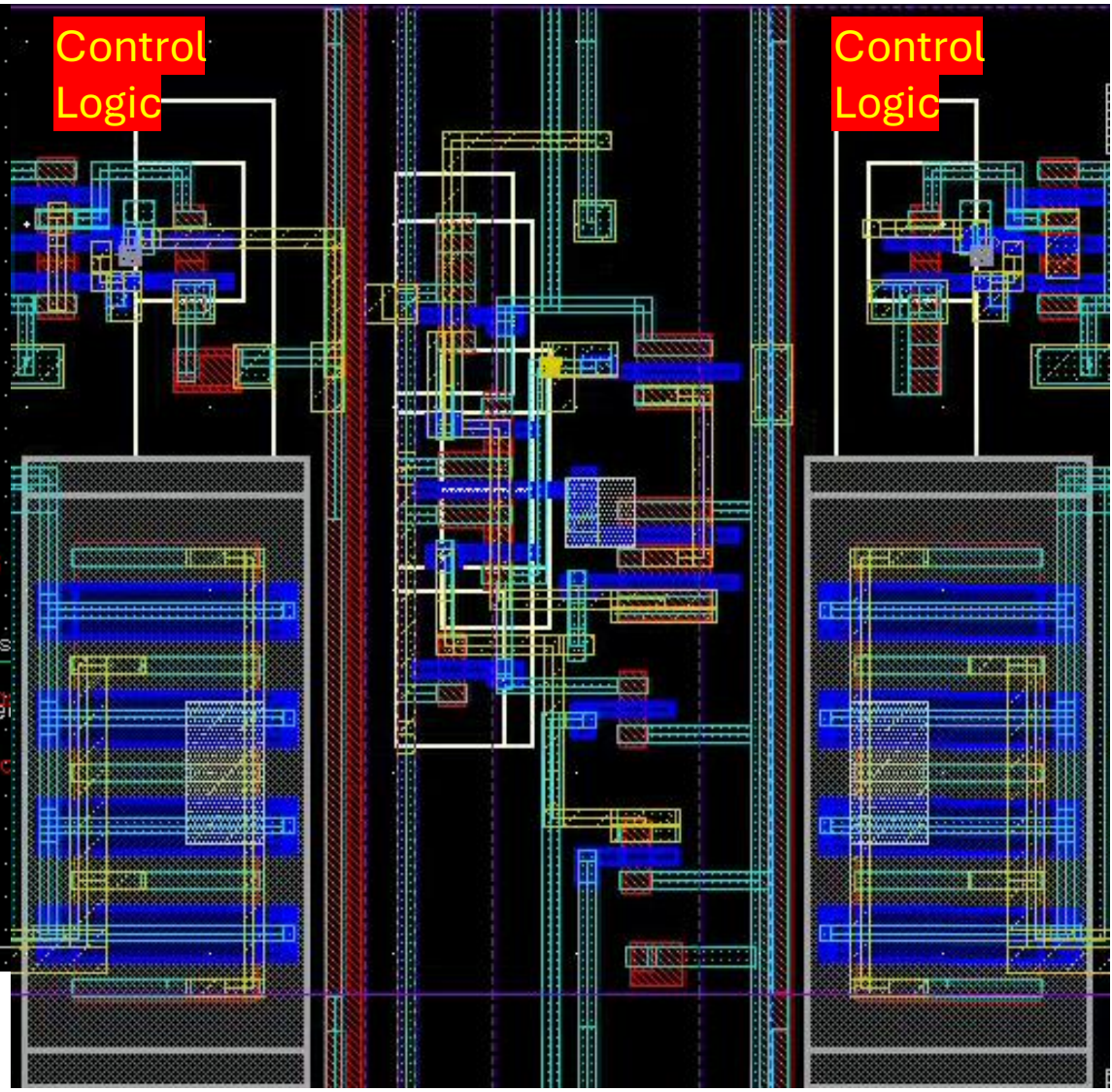


Operates at
CLK = 5GHz (Fast SCA Column)
CLK = 2.5GHz (Slow SCA Column)

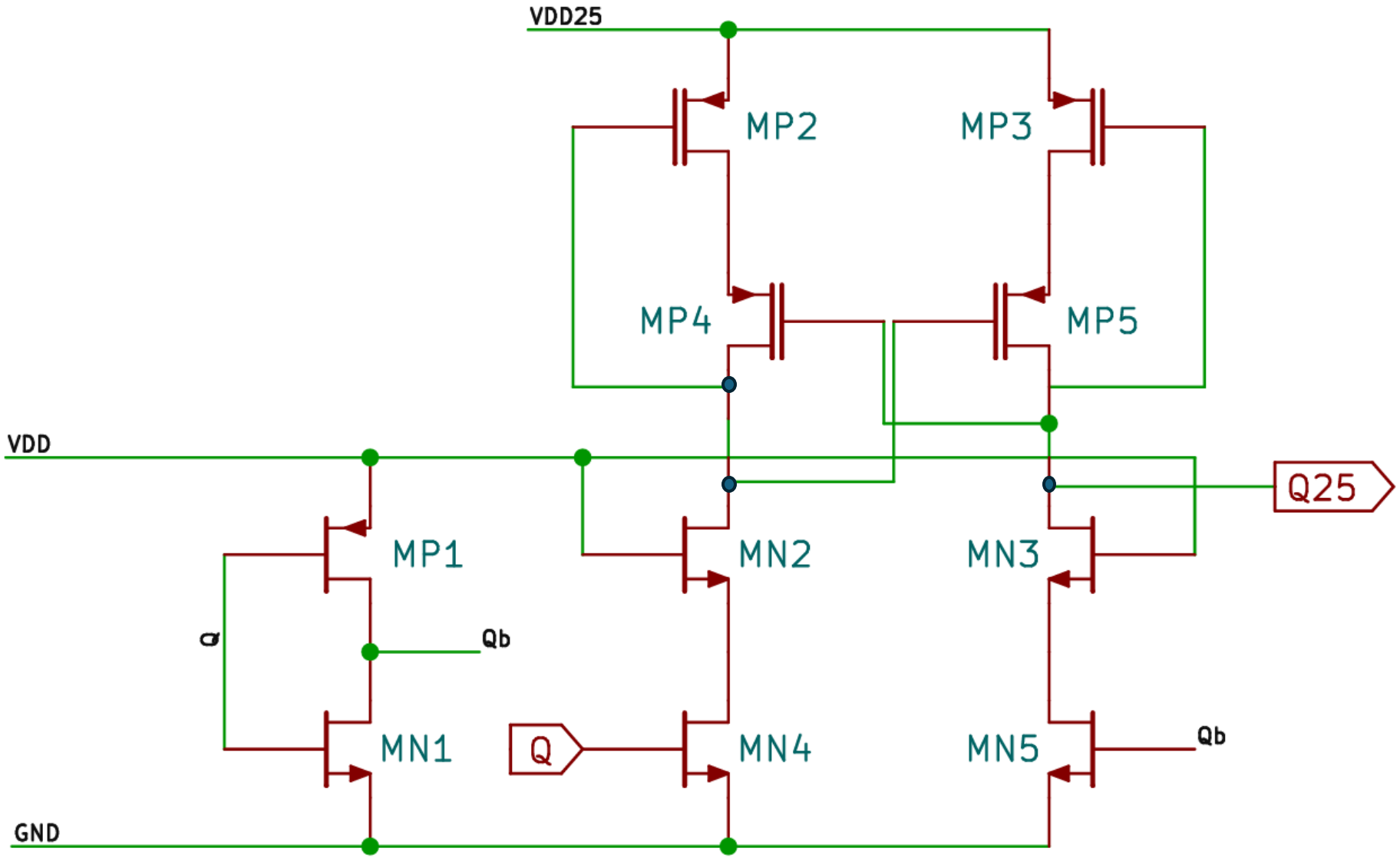


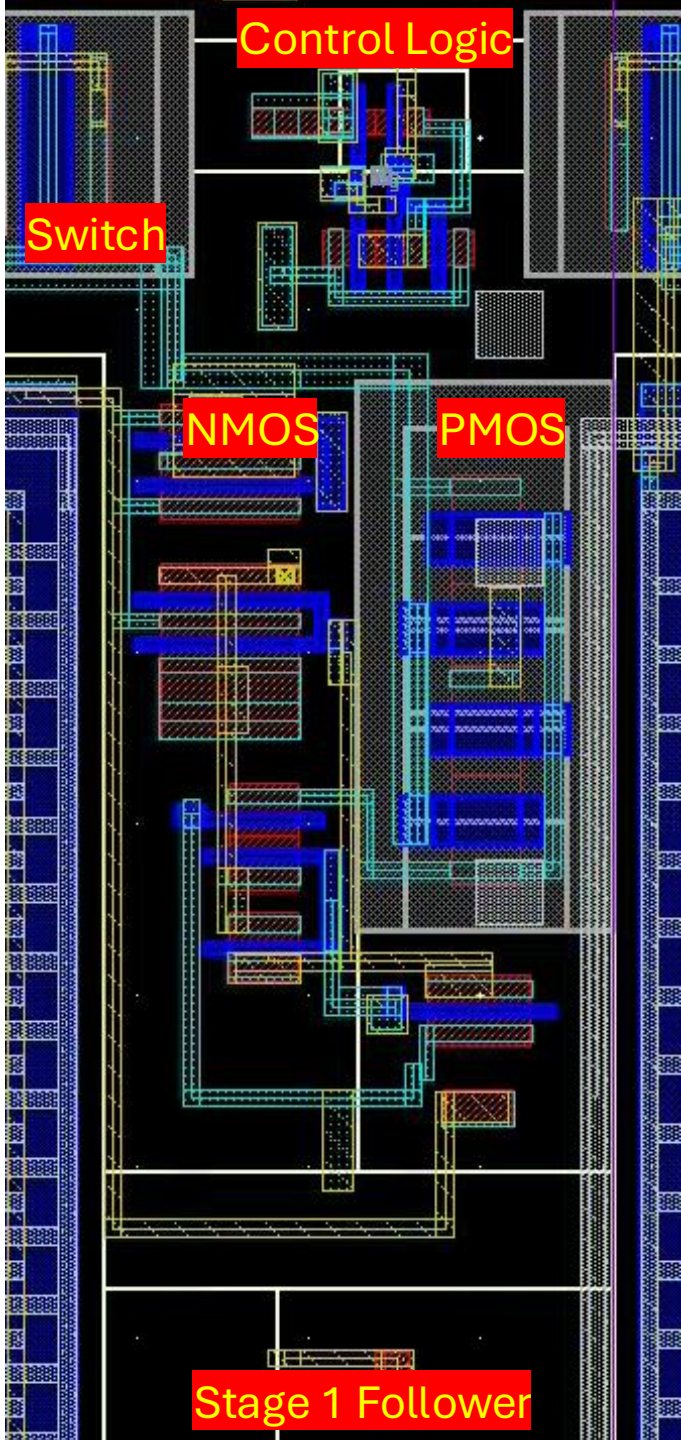
- Control Logic



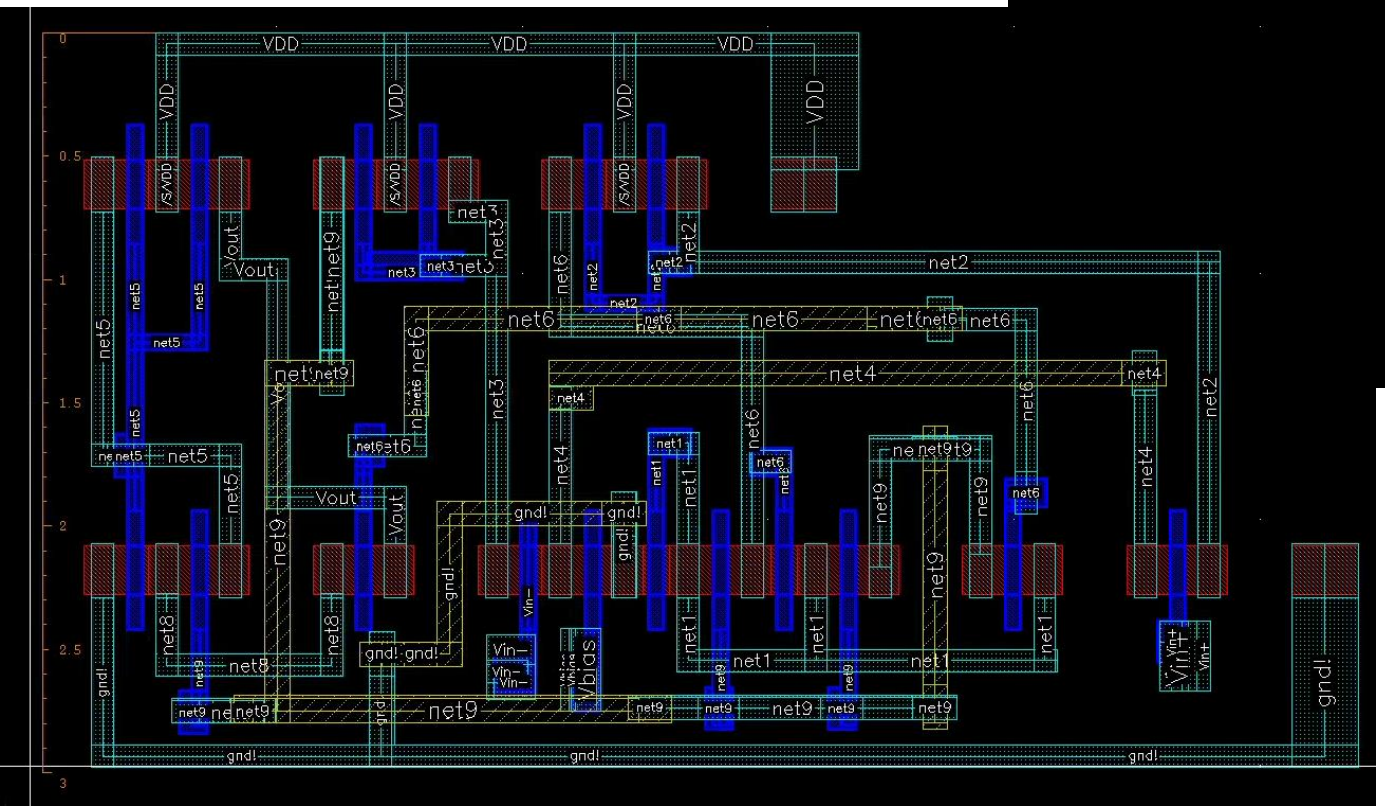


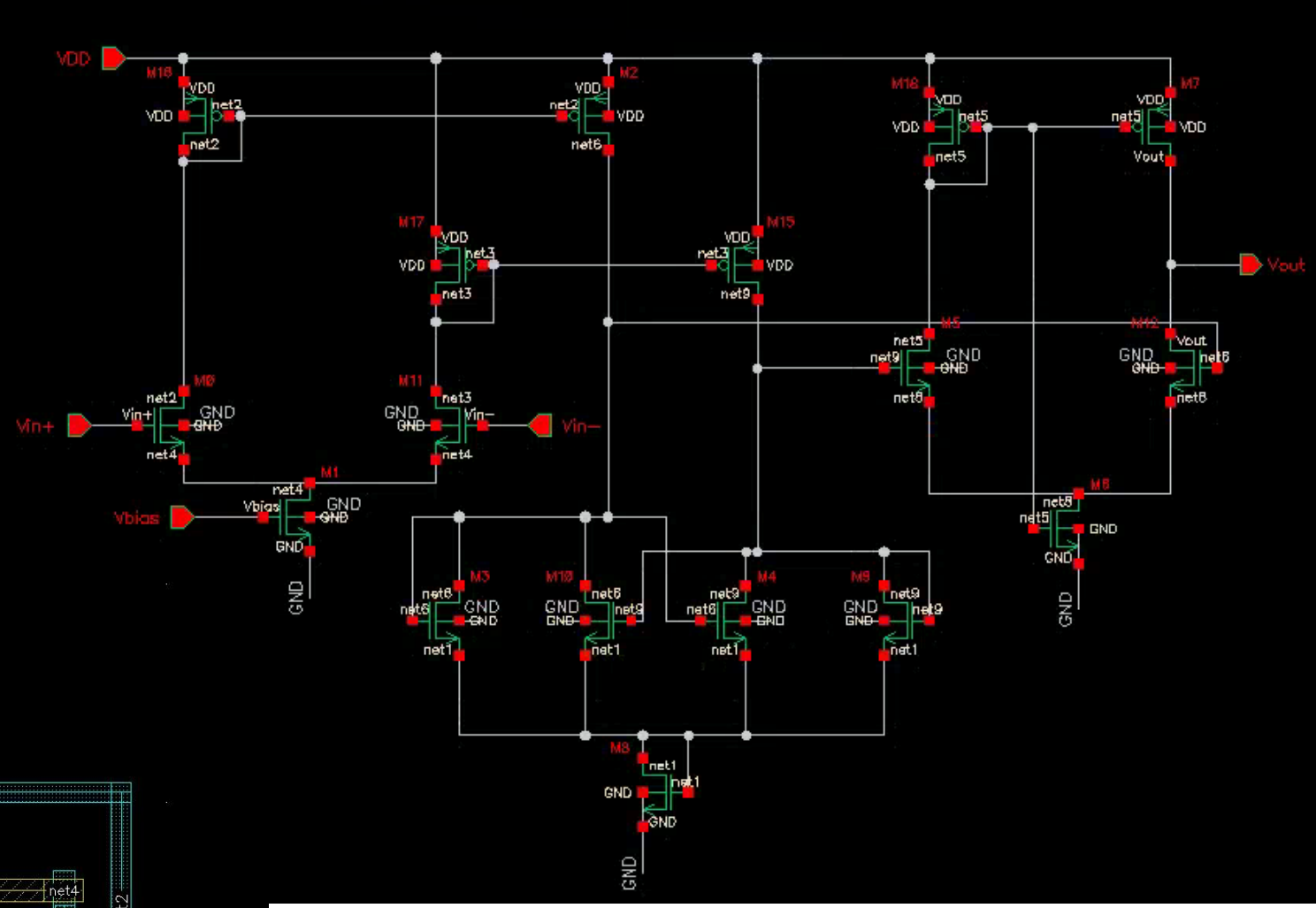
- 1.2V to 2.5V Voltage Level Shifter





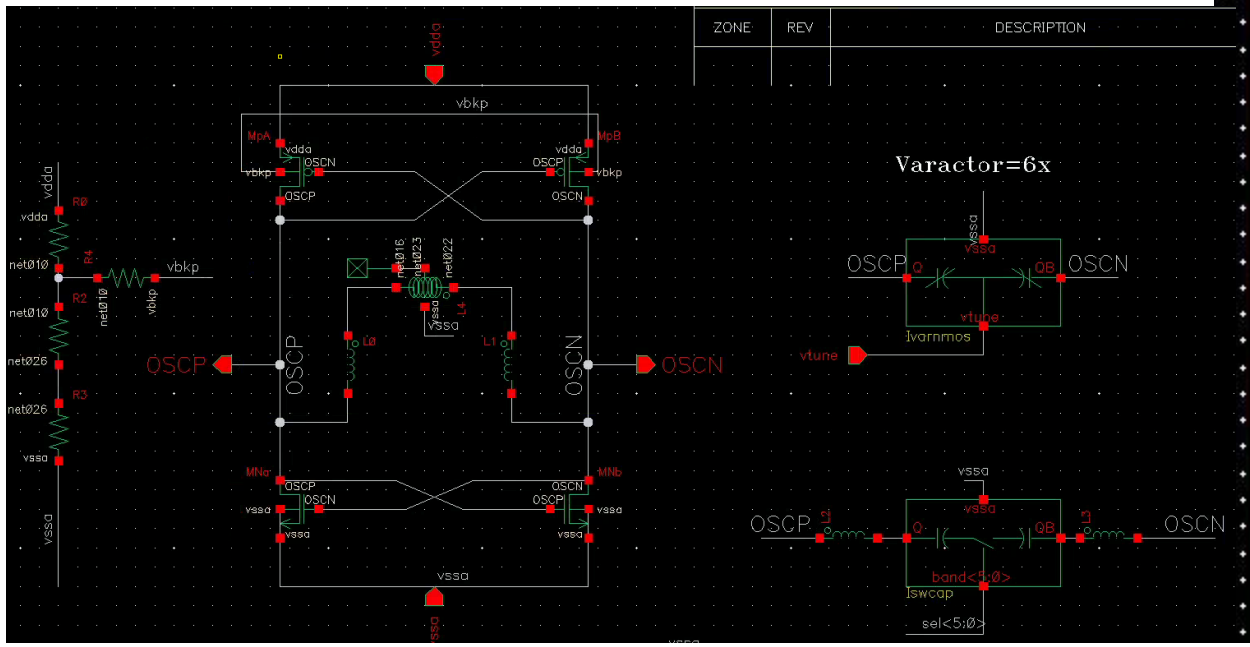
8. Discriminator

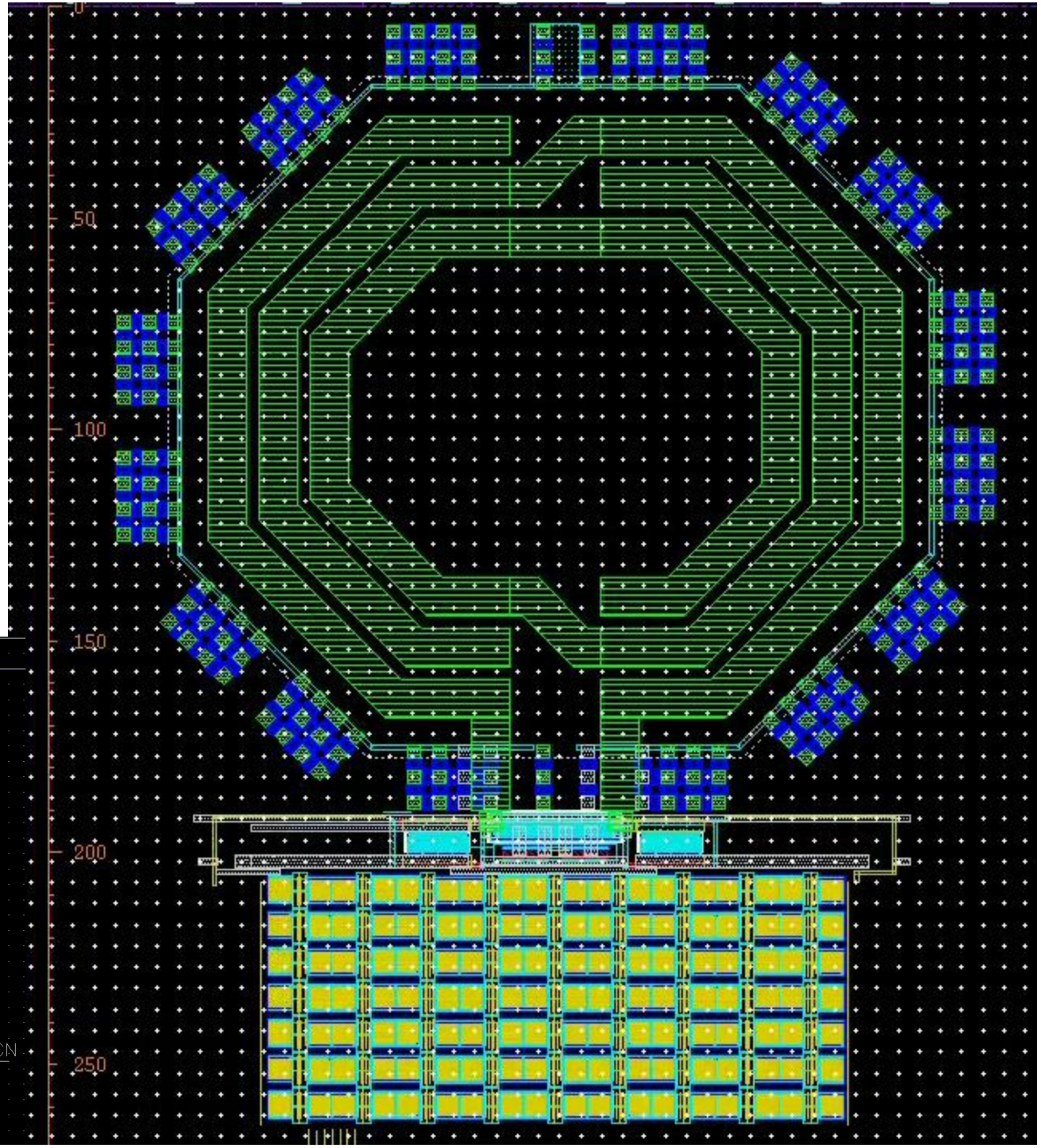




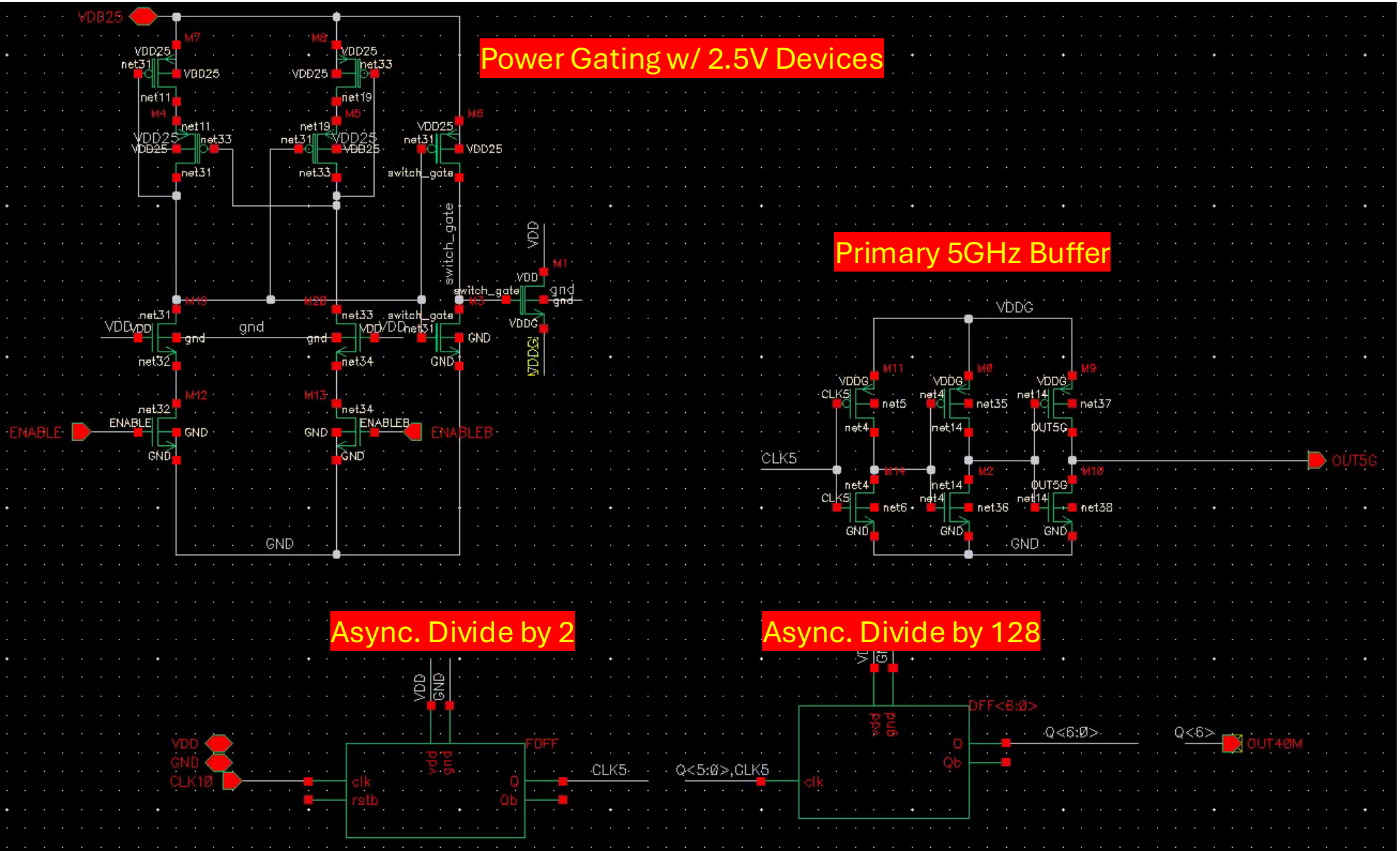
7. Clock Distribution

- 10 GHz VCO (Fermilab)
- Control Voltage is sourced from the FPGA to create a feedback loop.

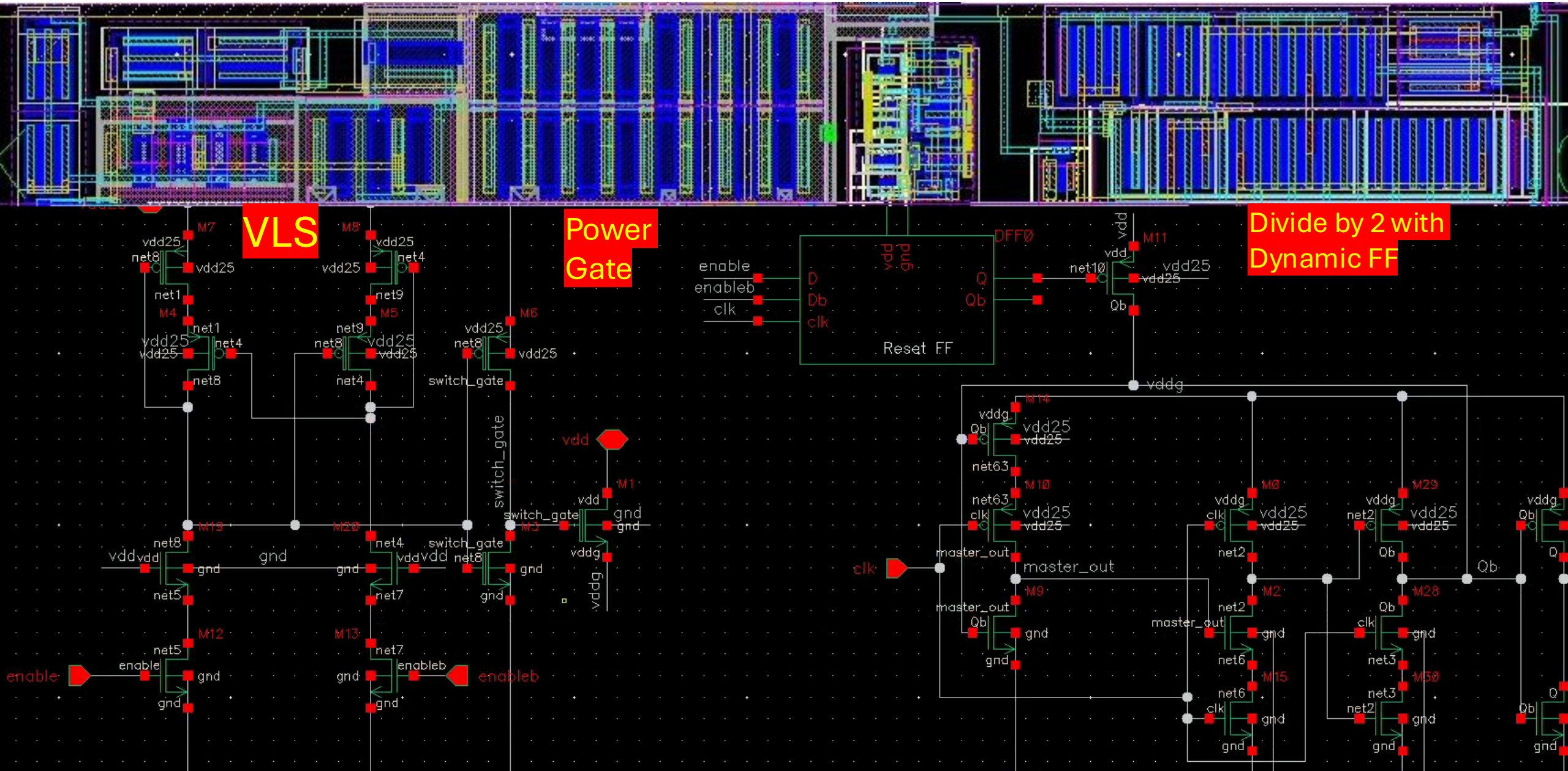




- Power Gated Primary Clock Buffer

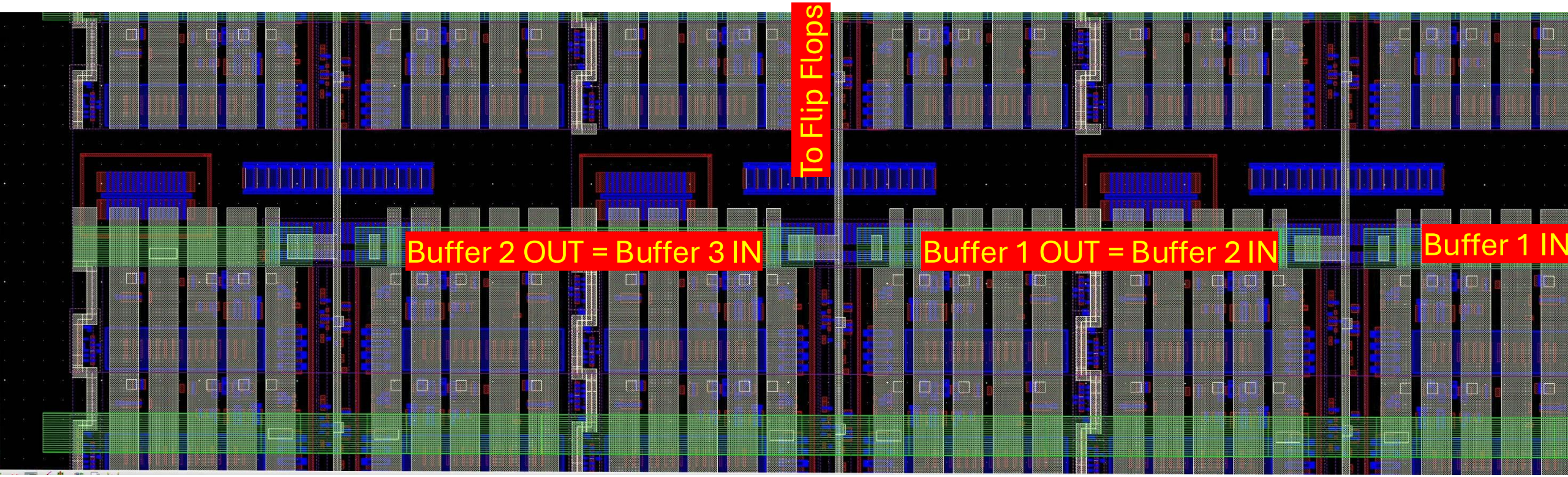


- Power Gated Secondary Clock Buffer



- 5GHz Clock Skew Generation

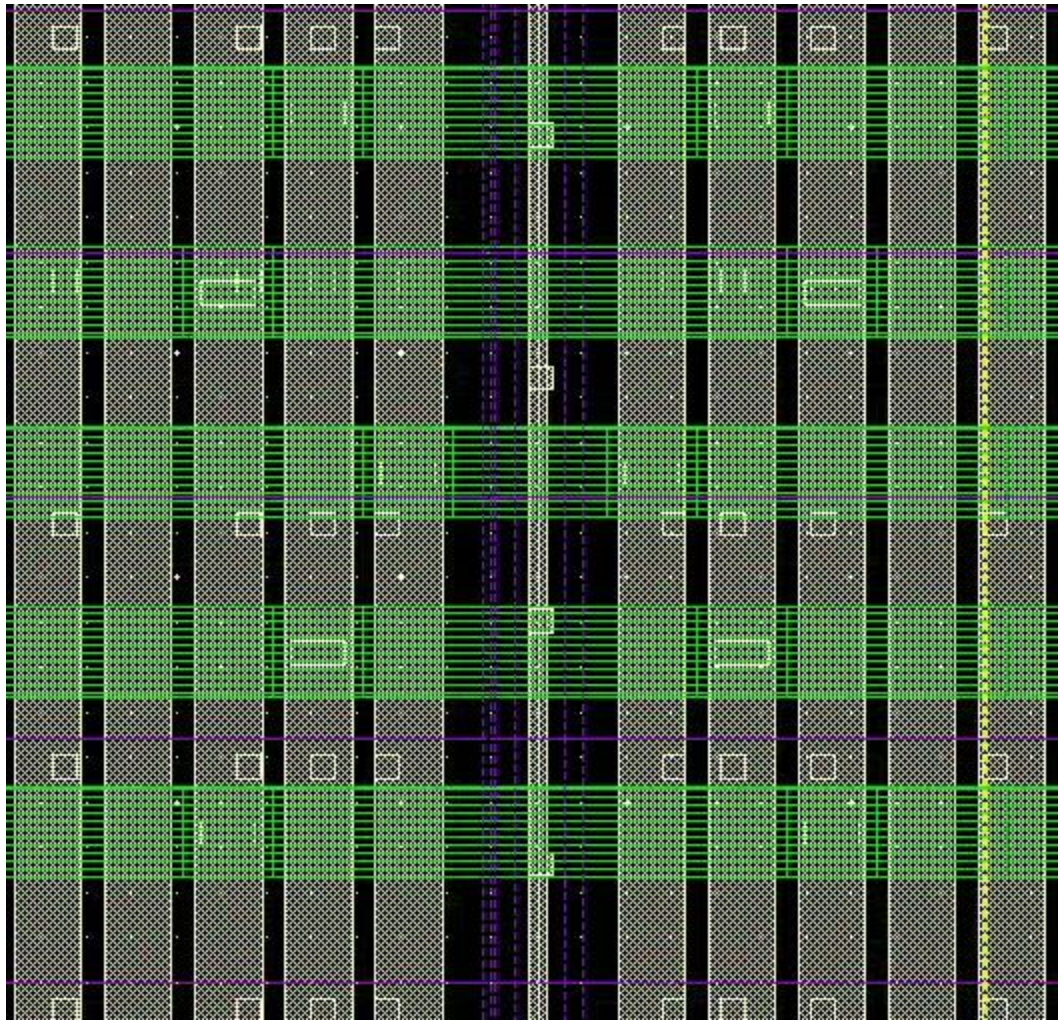
Buffers are sized so that it’s skew is 25ps in tt corner.



8. Power Distribution & Consumption

- M8(1.5μm wide, 2μm pitch)
- M9(2μm wide, 4μm pitch)
- VDD25, VDD, GND(Substrate)
- AVDD, AGND

	Worst Case	Best Case
Input Source Follower [mW/Ch]	9.2	4.0
SCA (Sampling) [mW/Ch]	16.6	13.9

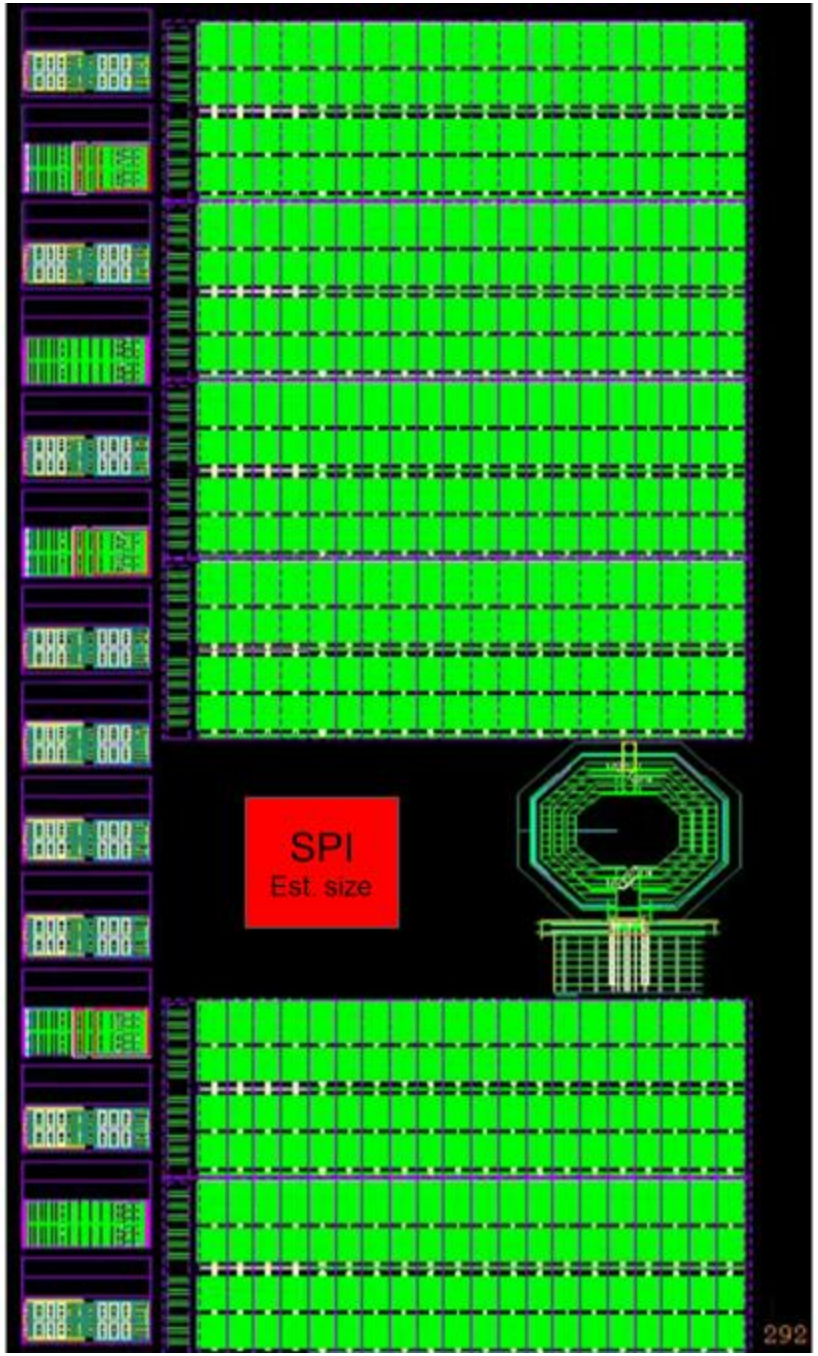


Overview

Register Address	Read/Write	Content	Description
0		Reserved	Will read out nothing
1	R/W	Trigger Channel Mask	0: Disabled, 1: Enabled
2	R/W	Instruction	1: Reset, 2: Readout, 3: Start
3	R/W	Mode	0: Use 1 Fast SCA bank to capture an edge, 1: Use 2, 2: Use 4
4-10	R	Counter 0 Values	last 6 bits of reg 10, 17, 24, 31, 38, 45, 52, 59 are not data
11-17	R	Counter 1 Values	
18-24	R	Counter 2 Values	
25-31	R	Counter 3 Values	
32-38	R	Counter 4 Values	
39-45	R	Counter 5 Values	
46-52	R	Counter 6 Values	
53-59	R	Counter 7 Values	

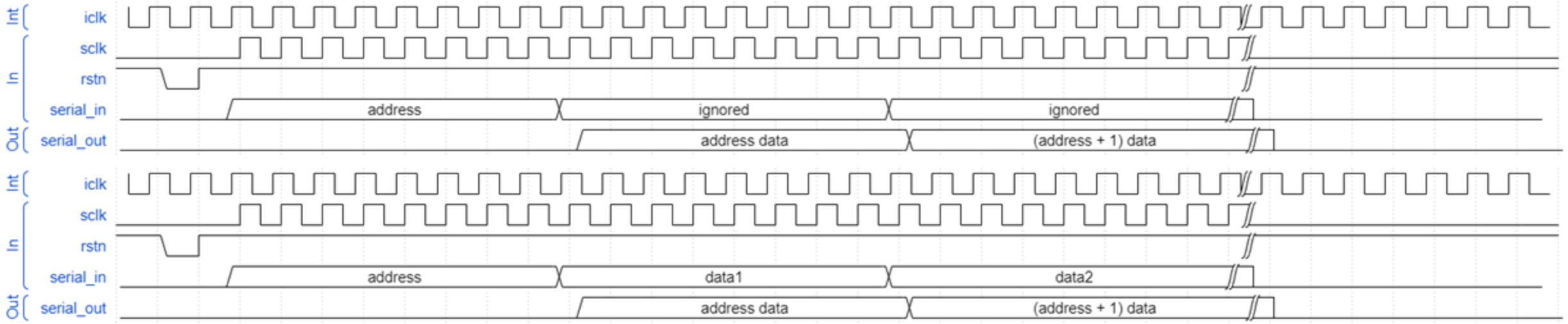
Table 1: SPI Register Map. All registers are 8 bits long.

- Two clock domains: SPI clk (~40-50 MHz) & Internal (~40 MHz)
- Takes string of bytes: first sets address, rest are data to write
- address increments every 8 SPI clk cycles

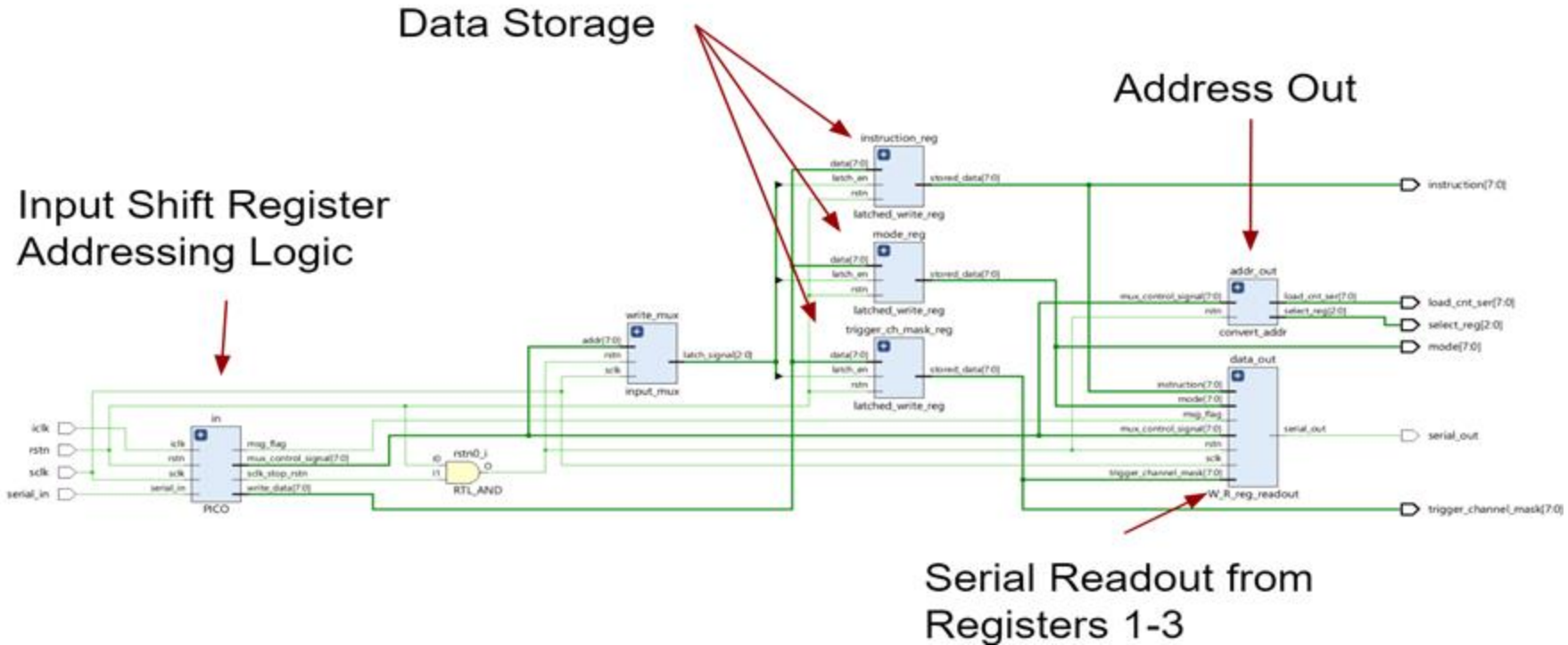


Schematic

Reading



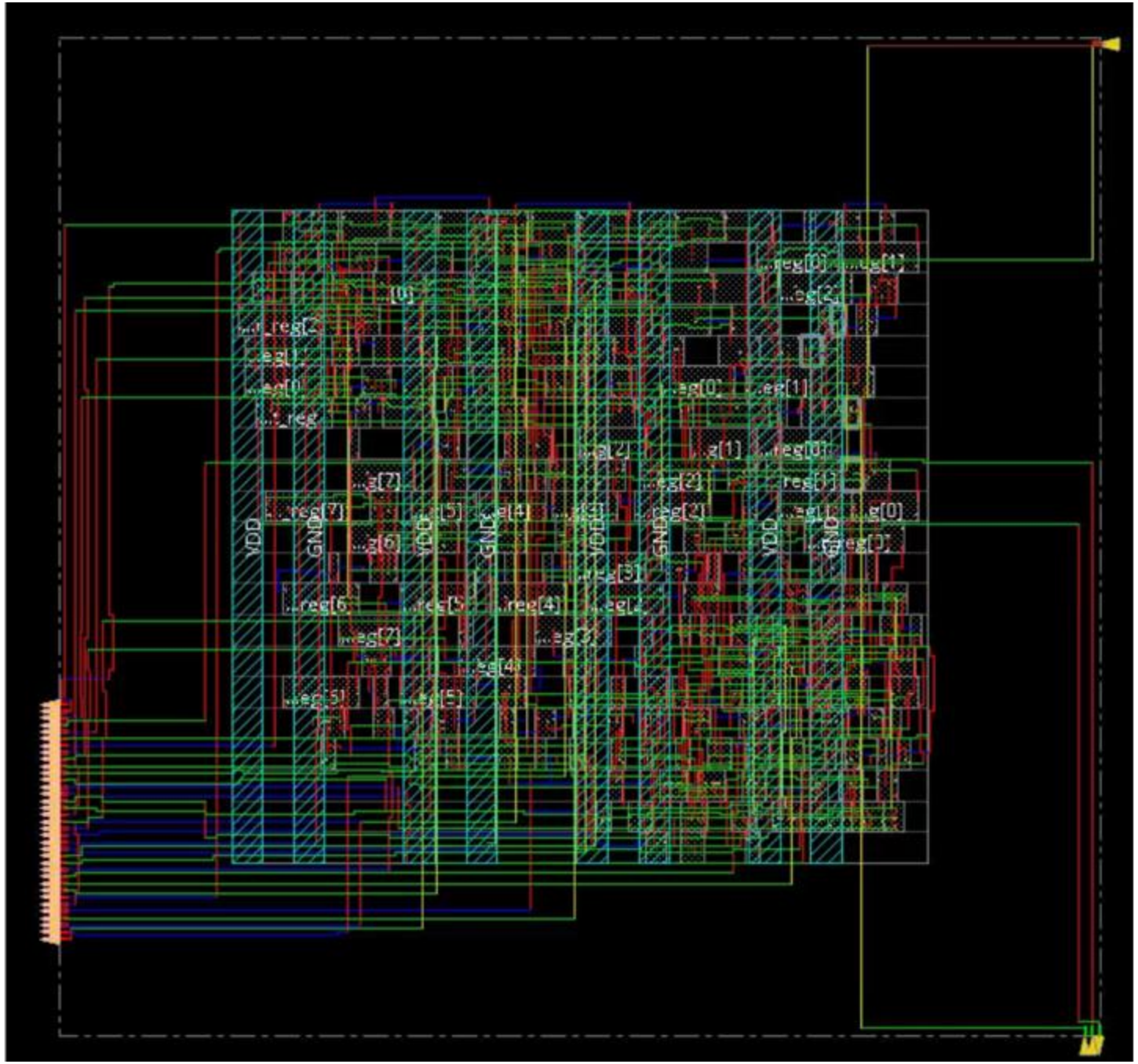
Writing



Layout

Total size:
60x60
um^2

Core size:
40x40
um^2



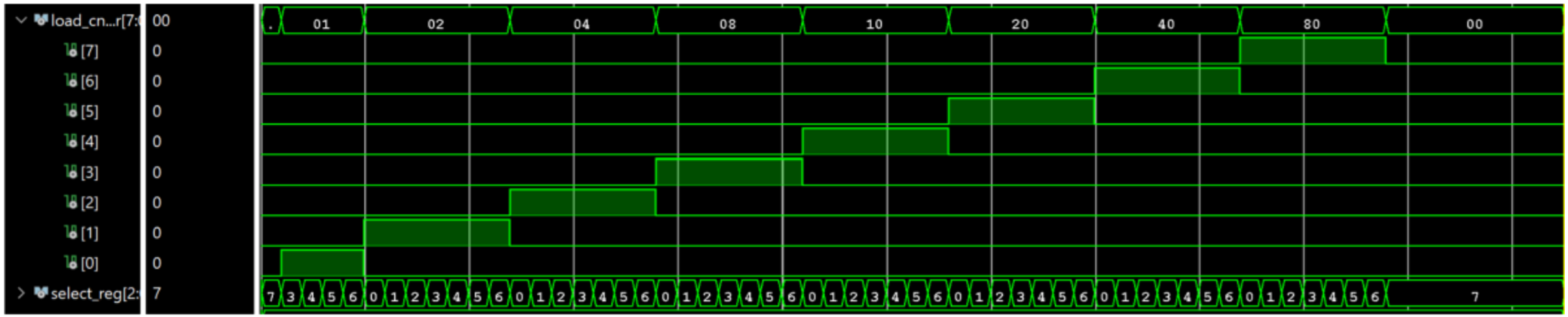
- Mode
- Instruction
- Trigger Channel Mask
- Load Count Ser
- Select Reg

- Rstn
- Internal Clock

- SPI clk
- Serial Out
- Serial In

Verification

- Data is cataloged by: Analog Channel, Channel Register
- Load_cnt_ser [8 bit]: Addresses the analog channels
- Select_reg [3 bit]: Addresses the register in a given analog channel
- Increments through registers in a given channel, then increments the channel



- Passed reading through all registers sequentially
- Passes reading and writing to special registers

Time Analysis

```
------------------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------------------

Setup views included:
 default

+--------------------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg |reg2cgate| default |
+--------------------+---------+---------+---------+---------+
|           WNS (ns):|  0.000  | 24.587  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |   N/A   |    0    |
|          All Paths:|   48    |   31    |   N/A   |   32    |
+--------------------+---------+---------+---------+---------+
```

*WNS: Worst Negative Slack
*TNS: Total Negative Slack

25ns period sclk; 23ns input delay; 2ns output delay
Synthesized clock tree for SPI clk and internal clk

Q: How to reset the address?
A: Wait for 7 iclk cycles without sending sclk. Then send another address.

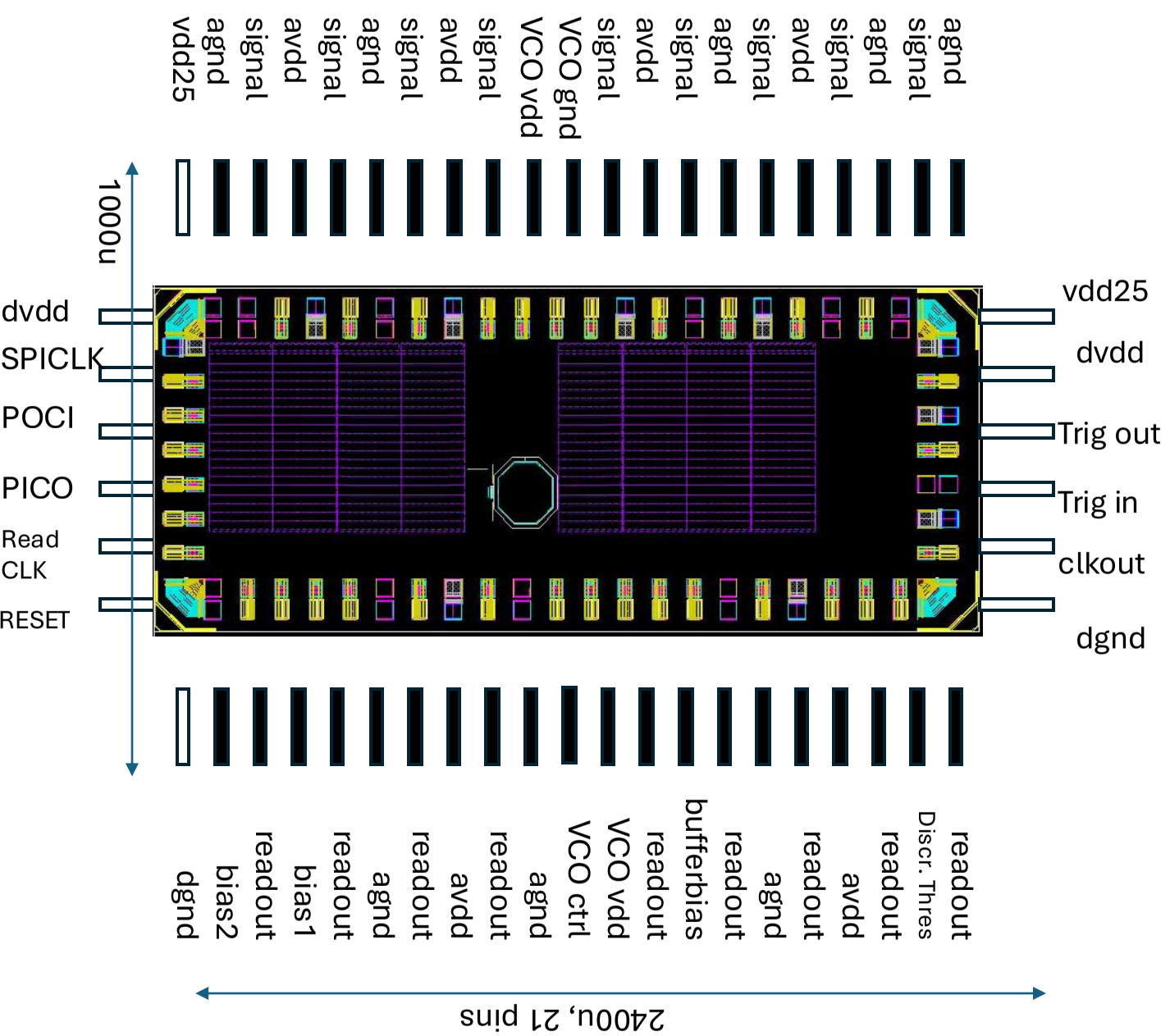
Q: What if an invalid address is sent?

A: load_cnt_ser <= 00000000, select_Reg <= 111. This means no data is read out.

Q: Is there any error correction?

A: We don’t have any. This shouldn’t be a problem.

Pin Layout (54 pins)



Executive Session

Analog

- Clock Skew Generation: Is it reliable? Is there a better way to do it?
- Inevitable clock skew between channels (O(10ps)): Will it affect the calibration?
- Signal Integrity: Is it reliable considering mismatch and process variation?

Executive Session

Application

- Length of a fast SCA bank (1.6 ns): Is it good for LAPPDs? What about other detectors?
- SCA banks can be used as 4* 1.6 ns, 2* 3.2 ns, or 1* 6.4 ns, where the multiplier means the number of edges captured within 208.4 ns window. Is this feature useful?
- Readout rate: Is 30kHZ event rate good enough? (w/ 40MHz readout clock)
- Do we need a feature which disables slow SCA bank readout? (156kHz) Do we need a feature which supports pipelined readout (simultaneous read/write) of four fast SCA banks? (625kHz)
- How high a readout clock frequency shall we support? (Currently 40MHz max due to RC, higher frequency bad for signal integrity.)

Executive Session

Digital

- What to do with the last 6 bits of the digital registers?
- Would the design benefit from running faster?
- How often should internal reset occur if no data is sent in?
- How to make sure a transaction is complete before starting the next one (how does one count 7 iclk cycles from the FPGA)?

Supplementary Slides

```
External Reset ------------------------
Writing to trigger channel mask: Passed
Writing to instruction: Passed
Writing to mode: Passed
Internal Reset ------------------------
select_reg on reg 4: Passed
load_cnt_ser on reg 4: Passed
select_reg on reg 5: Passed
load_cnt_ser on reg 5: Passed
select_reg on reg 6: Passed
load_cnt_ser on reg 6: Passed
select_reg on reg 7: Passed
load_cnt_ser on reg 7: Passed
select_reg on reg 8: Passed
load_cnt_ser on reg 8: Passed
select_reg on reg 9: Passed
load_cnt_ser on reg 9: Passed
select_reg on reg 10: Passed
load_cnt_ser on reg 10: Passed
select_reg on reg 11: Passed
load_cnt_ser on reg 11: Passed
select_reg on reg 12: Passed
load_cnt_ser on reg 12: Passed
select_reg on reg 13: Passed
load_cnt_ser on reg 13: Passed
select_reg on reg 14: Passed
load_cnt_ser on reg 14: Passed
select_reg on reg 15: Passed
load_cnt_ser on reg 15: Passed
select_reg on reg 16: Passed
load_cnt_ser on reg 16: Passed
select_reg on reg 17: Passed
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select_reg on reg 18: Passed
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select_reg on reg 20: Passed
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select_reg on reg 30: Passed
load_cnt_ser on reg 30: Passed
select_reg on reg 31: Passed
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load_cnt_ser on reg 56: Passed
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load_cnt_ser on reg 57: Passed
select_reg on reg 58: Passed
load_cnt_ser on reg 58: Passed
select_reg on reg 59: Passed
load_cnt_ser on reg 59: Passed
Internal Reset ------------------------
Reading from trigger channel mask: Passed
Reading from instruction: Passed
Reading from mode: Passed
```
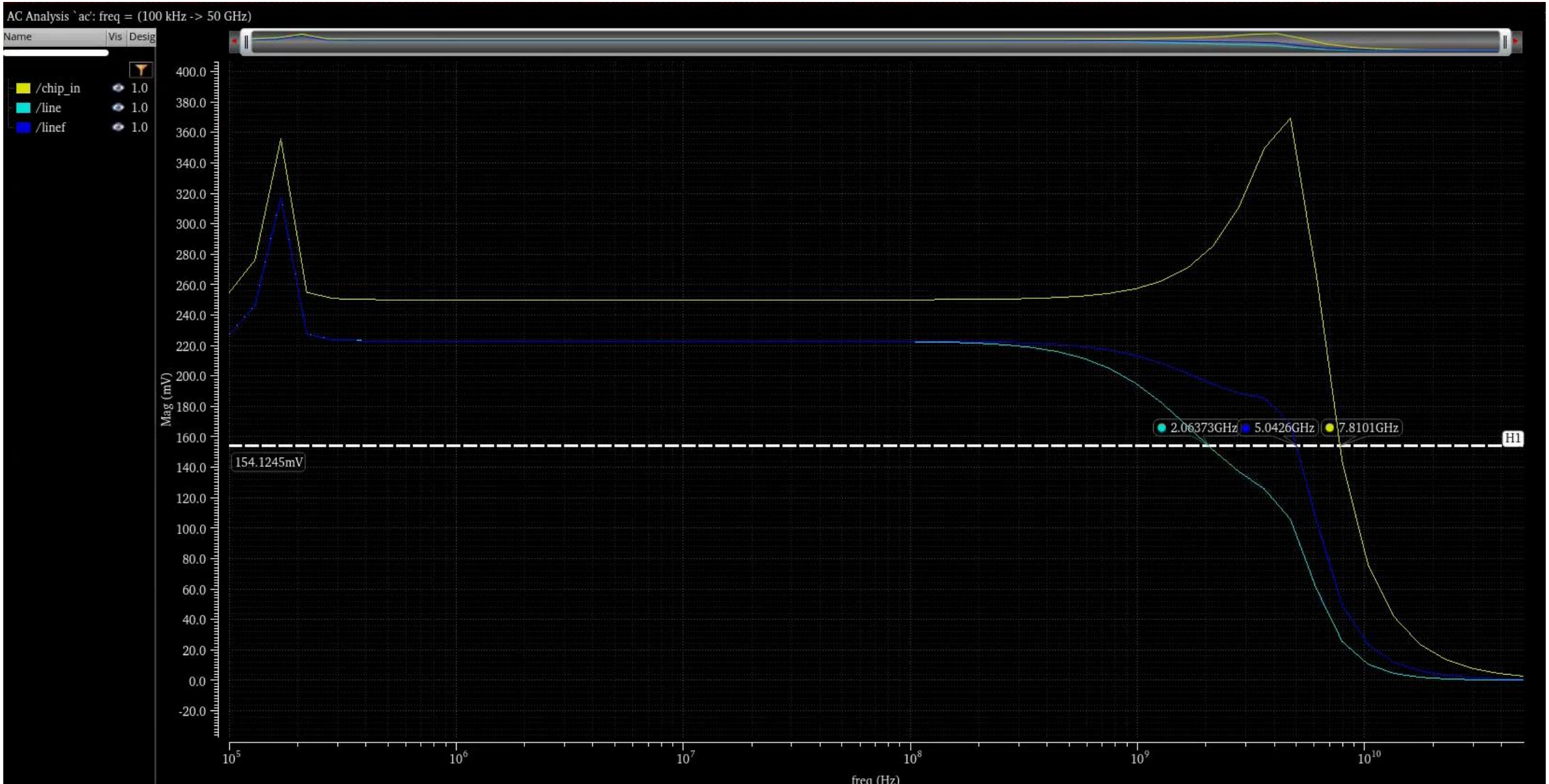
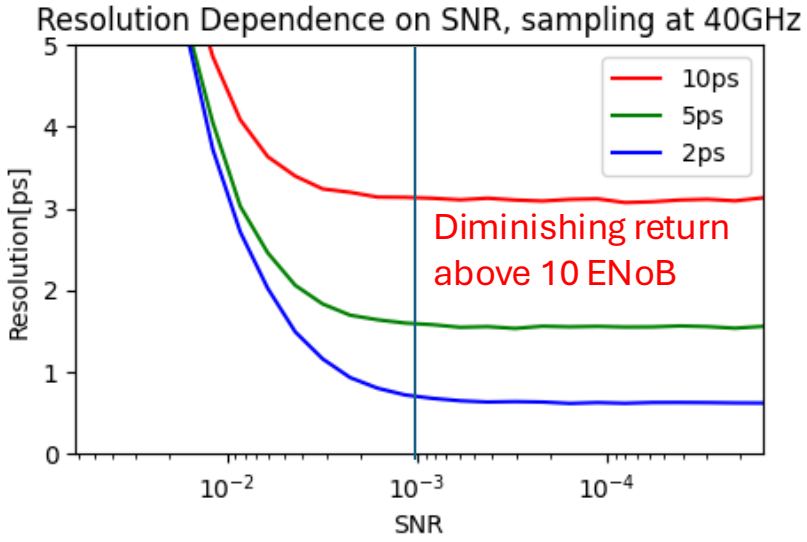
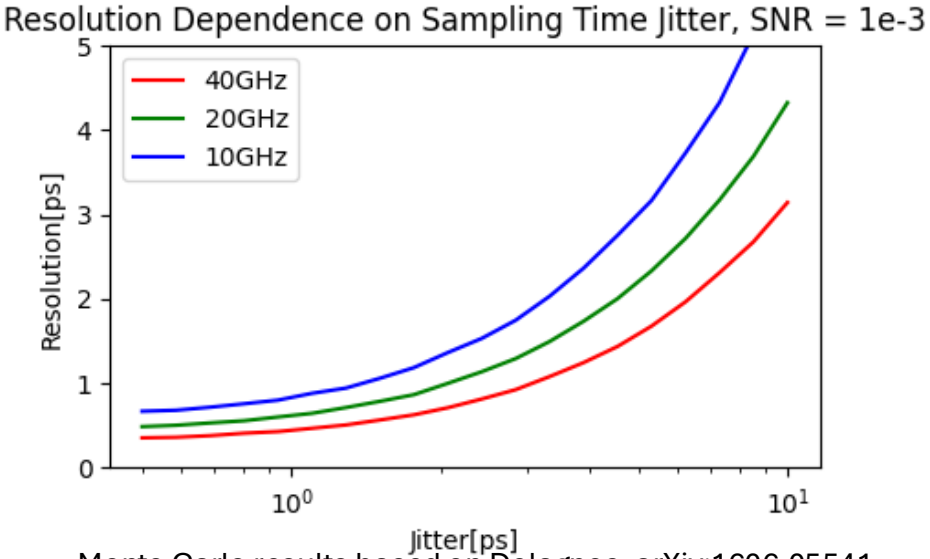

Analog BW


AC Analysis `ac': freq = (100 kHz -> 50 GHz)
Name
Vis
Desig
/chip_in 1.0
/line 1.0
/linef 1.0
Mag (mV)
freq (Hz)
2.06373GHz
5.0426GHz
7.8101GHz
H1
154.1245mV

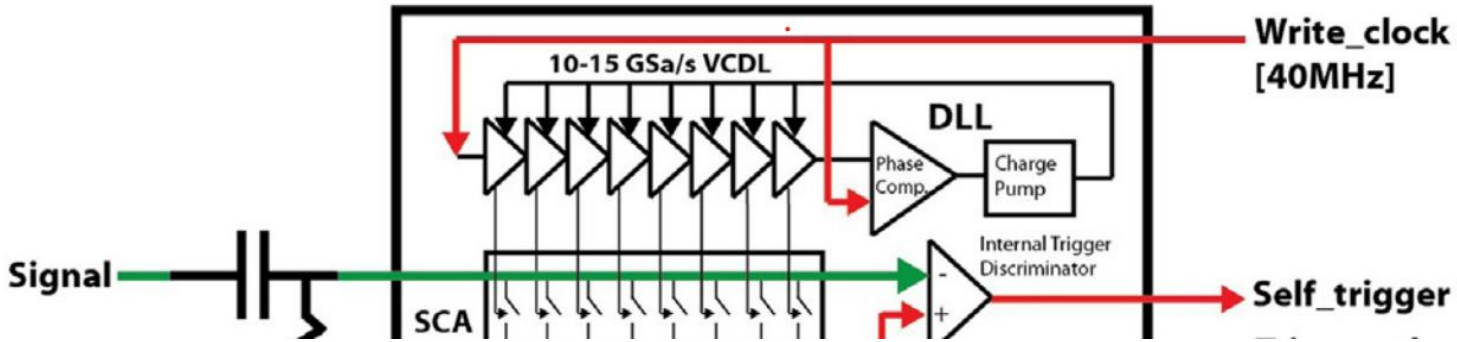
Point 2. Sampling Jitter





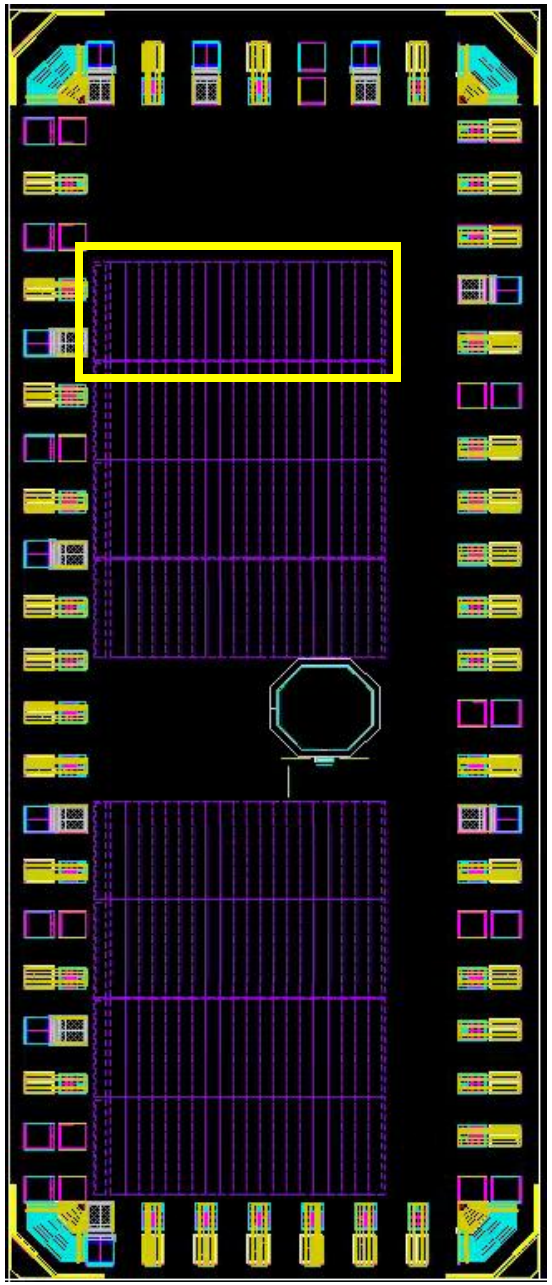
Monte Carlo results based on Delagnes, arXiv:1606.05541

- At <1ps timing resolution region, sampling jitter is a **dominant component** of the overall uncertainty.
- PSEC4 employs Delay Loop Lines (DLL) to control sampling switches.

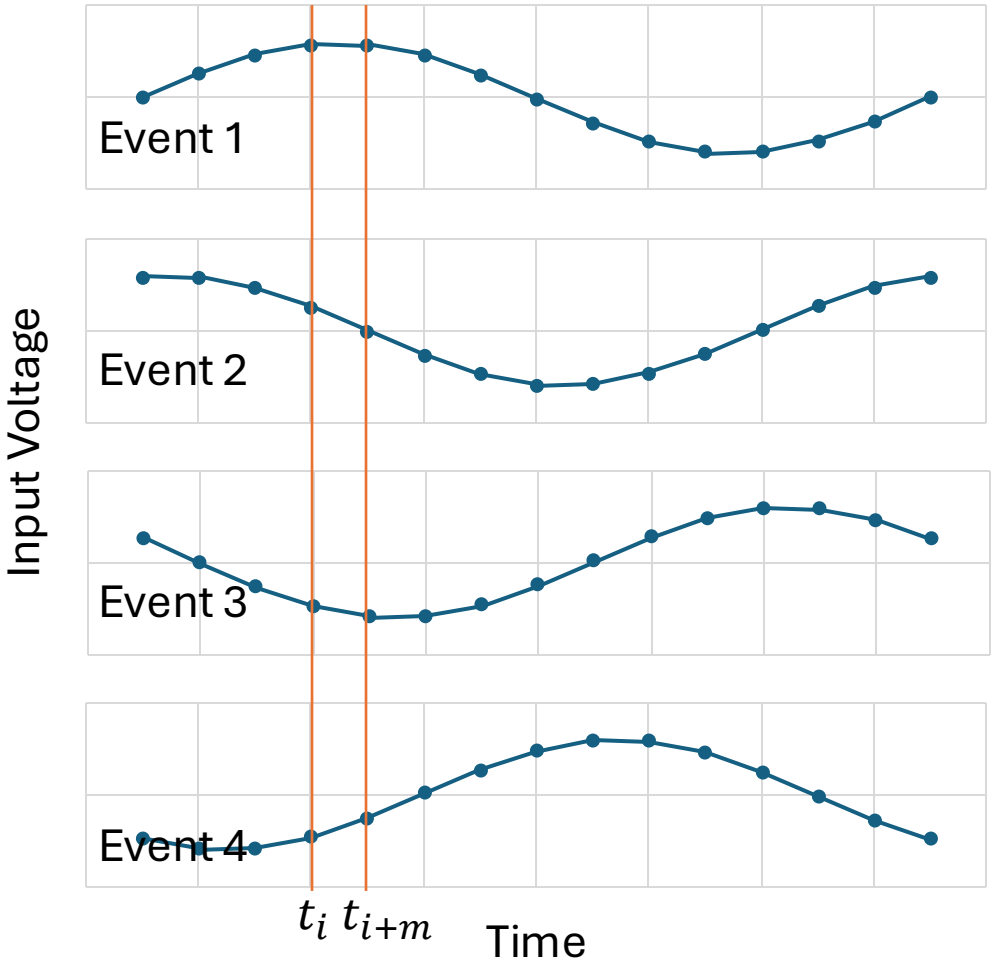


1 Sync Channel
+ 7 Normal Channels

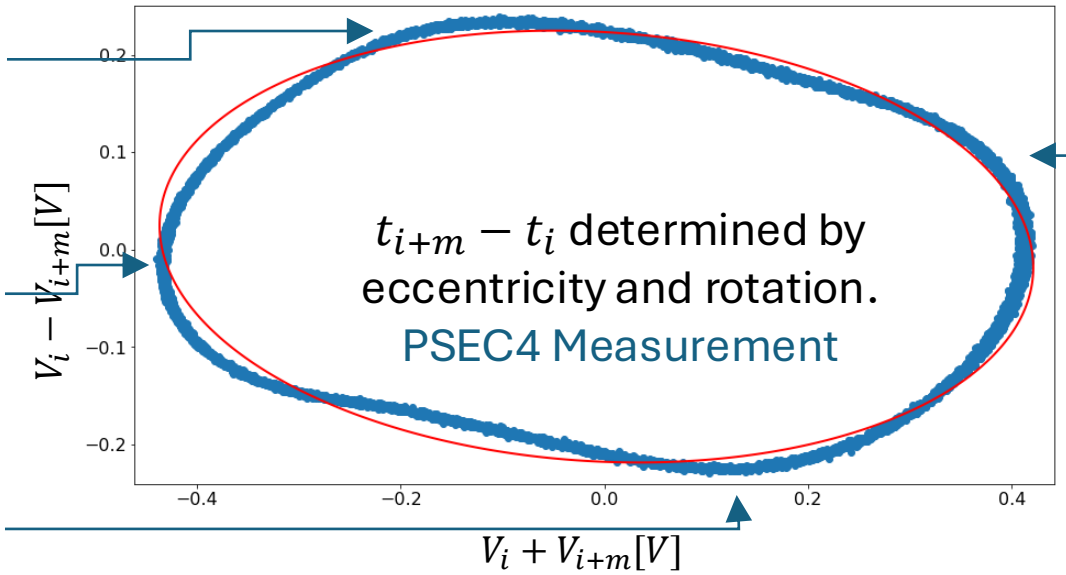
250MHz White Rabbit Sine Wave, synchronized across stations.



1. Measure many events of a sine wave.
2. Sum vs. Difference of two adjacent samples, over all events, form an ellipse.
3. Time offset can be determined from the coefficients.

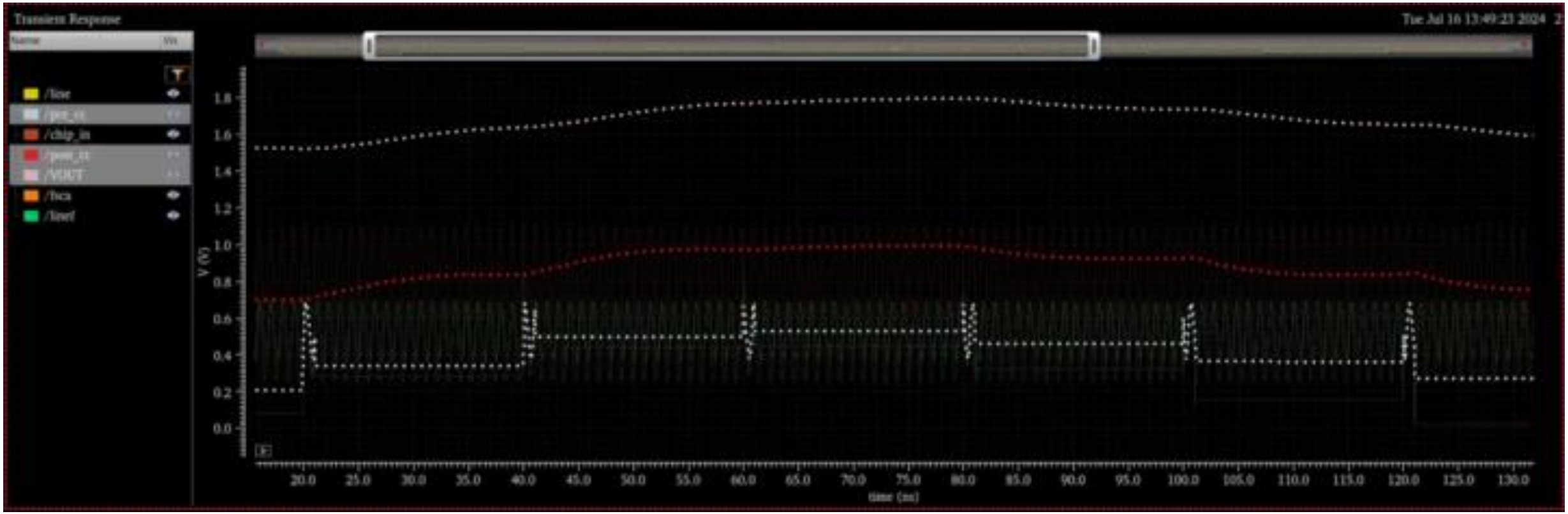


Bandwidth affects sample time uncertainty!

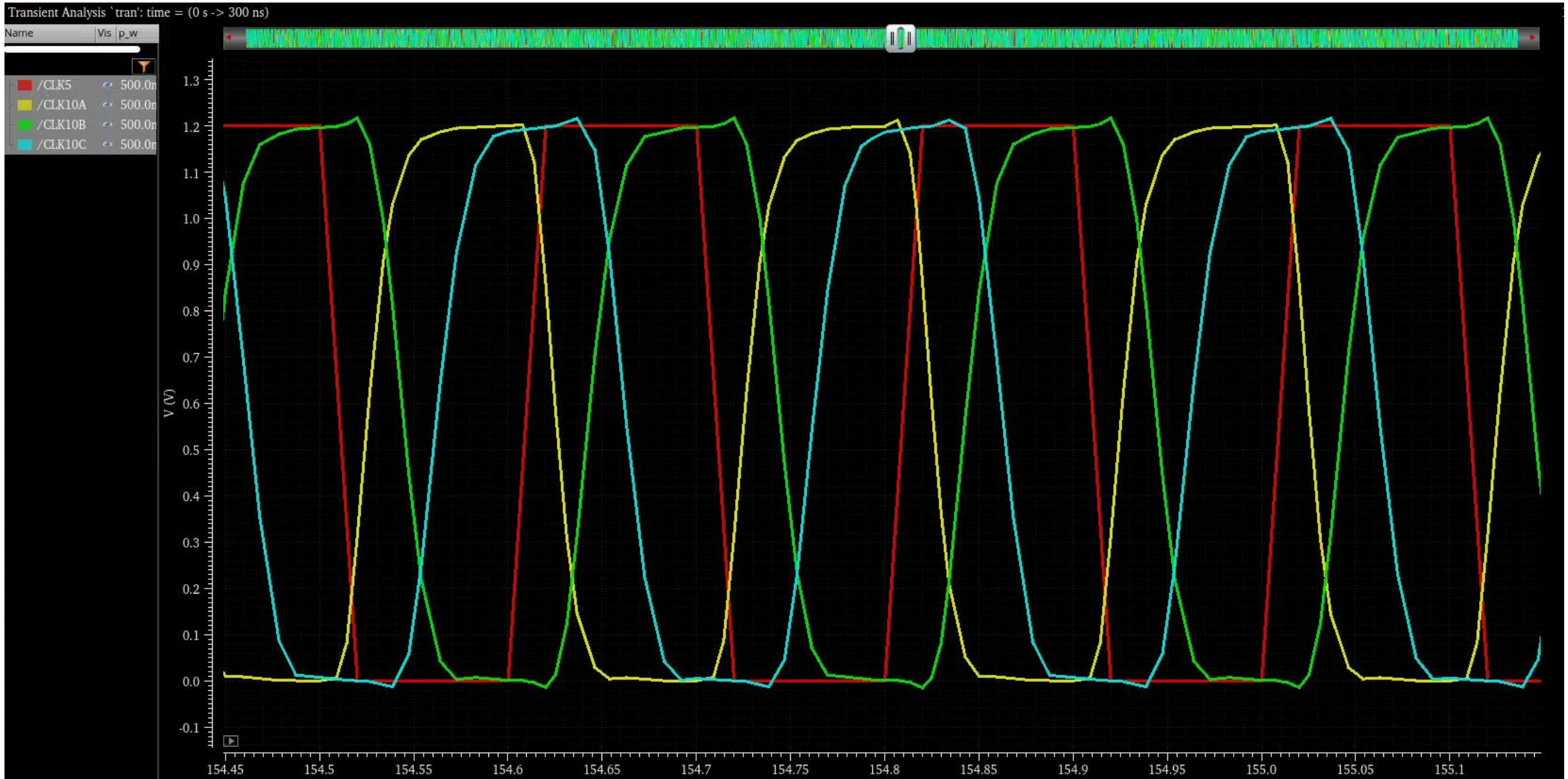


Low SNR → fainter, more spread curve.
Nonlinearity → distorted curve

Output Analog Characteristic



Clock Skew


Transient Analysis `tran': time = (0 s -> 300 ns)
Name
Vis
p_w
/CLK5
/CLK10A
/CLK10B
/CLK10C
500.0n
V (V)
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
-0.1
154.45
154.5
154.55
154.6
154.65
154.7
154.75
154.8
154.85
154.9
154.95
155.0
155.05
155.1