

PSEC5 Godparent Review Discussion Notes

Jinseo Park

Analog

Clock duty cycle is important when dual edge triggered flip flops are used.

- Clock buffers introduce duty cycle skews. (Xiaoran Wang)
- Dual Edge-triggered Flip Flops does not require the duty cycle to be 50%, but it will fail on the heavily skewed clock.

What is the operating frequency range of the clock divider?

- The 10GHz VCO can be tuned above 11GHz, which is above the operating frequency of the clock divider in ss corner. (Xiaoran Wang)
- What is the frequency range of the VCO?
- The clock divider is yet to be fully characterized over large frequency range.

Do you have to reset the clock divider?

- Since the subblock resets are synced to the 5GHZ clock, the 5GHz clock generator itself does not have to be reset
(Xiaoran Wang, Troy England)

Does the FPGA feedback loop for the VCO work?

- This is yet to be fully understood. (Xiaoran Wang)

What should be the maximal frequency of the readout clock?

- It does not matter, as this is a pathfinding chip. 40MHz is good enough. (Paul Rubinov, Henry Frisch)
- Similarly, various techniques to improve the readout rate is not applied.

Does the clock skew matter?

- The clock skew caused by long transmission lines are ok, as you can measure it and calibrate it. (Xiaoran Wang, Paul Rubinov)
- If the die gets larger, you can employ DLL to control the skew. (Xiaoran Wang)

Application

What is the number of channels?

- Currently 8, including the sync channel.
- It can be easily scaled up to 64, given enough die area and power.

What does the input pulse look like?

- Standard LAPPD pulse, SNR ~ 100 , Rise time 300 ps.

Does the trigger discriminate noises?

- Currently, trigger is generated by a simple comparator, which is good enough for LAPPDs.
- More complicated discrimination methods are required to use them for nano scintillators (Paul Lecoq)

Why is the 1 ps resolution relevant?

Time of Flight system using LAPPDs for Particle ID (Pion, Kaon)

- EIC: low momentum, but closer distance as well.
- LHCb
- KTEV

Digital

Our Questions

- What to do with the last 6 bits of the digital registers?
- Would the design benefit from running faster? Not really (Pastika)
- How often should internal reset occur if no data is sent in?
- How to make sure a transaction is complete before starting the next one (how does one count 7 iclk cycles from the **FPGA**)?

Reset does not have to be called many times because the standard cells are reliable.